TECHNICAL MANUAL

DIRECT SUPPORT AND GENERAL SUPPORT

MAINTENANCE MANUAL

FOR

MODEM, DIGITAL

DATA MD-920 A/G

(NSN 5820-00-155-8576)

This copy is a reprint which includes current pages from Changes 1.

HEADQUARTERS, DEPARTMENT OF THE ARMY

JUNE 1976

WARNING

HIGH VOLTAGE
is used in this equipment

DEATH ON CONTACT
may result if safety precautions
are not observed.

115 volts ac is present within the IFC modem. Perform all possible maintenance with power removed. If necessary to perform operations with covers removed and power on, be extremely careful to avoid contact with high voltage.

DON'T TAKE CHANCES!

Technical Manual
No. 11-5820-804-34
Technical Publication
NAVELEX 0969-LP-169-4021
Technical Order
TO 31R5-2G-272

DEPARTMENTS OF THE ARMY,

THE NAVY, AND THE AIR FORCE

WASHINGTON, DC 8 June 1976

DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL FOR MODEM, DIGITAL DATA MD-920A/G (NSN 5820-01-057-6356)

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CHAPTER 1
INTRODUCTION

1-1. Scope

This manual contains necessary information for troubleshooting, repair and maintenance of Modem, Digital Data MD-920A/G, hereafter referred to as the ICF modem. Chapter 2 provides a detailed explanation of circuit operation. Direct support troubleshooting and maintenance procedures for the ICF modem are provided in chapter 3 and chapter 4 provides information for general support maintenance of the ICF modem. Chapter 5 provides necessary information for the modem power supply, including functional description, maintenance, repair, and troubleshooting. Appendix A contains references, appendix B contains wire lists, and appendix C defines mnemonics used on diagrams.

NOTE

Refer to TM 38-750 for Forms and Records, TM 750-224-2 for Destruction of Army Materiel to Prevent Enemy Use, and TM 740-90-1 for Administrative Storage.

1-2. Indexes of Publications

a. DA Pam 310-4. Refer to the latest issue of DA Pam 310-4 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

b. DA Pam 310-7. Refer to DA Pam 310-7 to determine whether there are modification work orders (MWO's) pertaining to the equipment.

1-3. Equipment Designators

Throughout this manual, assemblies and subassemblies are identified by reference designation; e.g., A2A1, A2A1A1, etc. These designators are the same as those marked on the equipment. The maintenance allocation chart in TM 11-5820-804-12 and the repair parts and special tools lists in TM 115820-804-20P and 34P are, however, organized in functional group code (FGC) sequence. To facilitate use of all equipment documentation, a reference designation to functional group code cross reference index is provided in table 1-1.

Table 1-1. Reference Designation/FGC Cross Reference

Reference designator	*Name*	*Assembly number*	*Functional group*
	Modem, MD-920A/G.	SM-D-759601	00
A1	Control Panel	SM-D-759656	01
A1A1	Switch Assembly.	SM-D-742008	0101
A1A2	Switch Assembly.	SM-D-742008	0102
A2	Modem Assembly	SM-D-759658	02
A2A1	Synthesizer and Bit Sync Assembly	SM-D-759603	0201
A2A1A1A1	Counter Encoder.	SM-D-742105	020101
A2A1A1A2	Programmable Divider.	SM-D-742109	020102
A2A1A1A3	Reference Oscillator.	SM-D-742129	020103
A2A1A1A5	Reference Divider.	SM-D-742133	020104
A2A1A1A6	45 MHz Phase Lock Loop.	SM -D-742113	020105
A2A1A1A8	45 MHz Amplifier.	SM-D-742117	020106
A2A1A1A10	Mixer/Output Amplifier.	SM-D-74125	020107
A2A1A1A11	15 MHz Amplifier.	SM-D-742121	020108
A2A1A1A12	Stable Clock	SM-D-731201	020109
A2A1A1 A14	Reference Divider.	SM-D-742133	020110
A2A1A1A15	Digital A1 To Analog Converter	SM-D-731217	020111
A2A1A1A16	Loop Filter	SM-D-731221	020112
A2A1A1A17	Transmit Bit Detector .	SM-D-742045	020113
A2A1A1A21	Line Driver	SM-D-742053	020114
A2A1A1A22	Line Driver	SM-D-742053	020115
A2A1A1A23	Line Driver	SM-D-742053	020116
A2A1A2A1	LOS/Cable Receiver and Decoder	SM-D-742089	020117
A2A1A2A2	NRZ Interface	SM-D-877791	020118
A2A1A2A3	LOS/Cable Driver	SM-D-742081	020119
A2A1A2A4	Input Interface .	SM-D-742037	020120
A2A1A2A5	Coder Interface .	SM-D-742049	020121
A2A1A2A6	Coder Switch	SM-D-742041	020122

Table 1-1. Reference Designation/FGC Cross Reference -Continued

Reference designator	*Name*	*Assembly number*	*Functional group*
A2A1A2A7	11-Bit PN Sequence Generator	SM-D-742057	020123
A2A1A2A8	Error Comparator	SM-D-742061	020124
A2A1A2A9	D/A Meter	SM-D-742065	020125
A2A1A2A10	Alarm Circuits	SM-D-742033	020126
A2A1A2A11	Transmit Bit Detector	SM-D-742045	020127
A2A1A2A112	Loop Filter	SM-D-731221	020128
A2A1A2A13	Digital To Analog Converter	SM-D-731217	020129
A2A1A2A14	15 MHz Amplifier	SM-D-742121	020130
A2A1A2A15	Mixer,/Output Amplifier	SM-D-742125	020131
A2A1A2A16	45 MHz Amplifier	SM-D-742117	020132
A2A1A2A18	45 MHz Phase Lock Loop .:	SM-D-742113	020133
A2A1A2A20	Reference Divider	SM-D-742133	020134
A2A1A2A21	Reference Oscillator	SM-D-742129	020135
A2A1A2A23	Programmable Divider	SM-D-742109	020136
A2A1A2A24	Counter Encoder	SM-D-742105	020137
A2B1	Blower	SM-A-731252	0202
A2B2	Blower	SM-A-731252	0203
A2PS1	Power Supply	SM-C-759630	0204
A2PS1A1	Transformer Assembly	SM-C-882244	020401
A2PS1A2	Printed Circuit Board	SM-D-882232	020402
A2PS1A3	Circuit Card Assembly	SM-C-882239	020403
A2PS1A4	Component Board Assembly Number 1	SM-C-882245	020404
A2PS1A5	Component Board Assembly Number 2	SM-D-882247	020405
A2PS1A6	Heat Sink Assembly Number 1	SM-D-882249	020406
A2PS1A7	Heat Sink Assembly Number 2	SM-D-882251	020407
A2PS1A8	Heat Sink Assembly Number 3	SM-D-882253	020408
A2PS1A9	Terminal Board Assembly	SM-C-882255	020409
A2PS1A10	Rectifier Assembly	SM-C-882257	020410
A2W2	Cable	SM-D-759631	0205
A2W3	Cable	SM-D-759632	0206
A2W9	Cable	SM-C-742193	0207
A2W11	Cable	SM-D-759654	0208
A2Y1	Oscillator	SM-A-731369-1	0209
A2Y2	Oscillator	SM-A-731369-1	0210

CHAPTER 2
FUNCTIONING OF EQUIPMENT

2-1. General

a. This chapter contains a description of the functioning of the ICF modem. A functional block diagram description of the entire modem is followed by detailed descriptions of each functional block in the modem. The supporting detailed card descriptions are grouped by function; i.e., bit synchronizer, synthesizer, etc.

b. Supporting illustrations such as block diagrams and timing diagrams are included within this chapter. Oversize functional block diagrams are shown in figures FO-1, FO-2, and FO-3.

c. The system applications of the ICF modem are explained in the following publications:

TM 11-5820-803-12	Operator's and Organizational Maintenance Manual for Modem, Digital Data MD-921/G
TM 11-5820-804-12	Operator's and Organizational Maintenance Manual for Modem, Digital Data MD-920A/G.

2-2. Functional Description

a. General. The ICF modem (fig. 2-1) provides a means of interfacing digital data over a shielded cable or line-of-site (LOS) microwave link by converting between baseband data signals and bipolar NRZ signals. The modem also provides for the interfacing of digital data over a fiber-optic (FO) cable link by converting between baseband data signals and an NRZ signal format. The modem will process data at any rate between 19.200 kb/s and 5.000 Mb/s. Self-test, link test, and on-line fault monitoring functions are built into the modem. External error-correcting coders/decoders (such as Encoder/ Decoder KY-801/GSC (NSN 5895-01-034-1061) [NAVELEX 0967-LP-594-2010; TO 31R5-2GSC1011 may be employed to improve the quality of communications. The modem has independent transmit and receive sections. The transmit section accepts a baseband data input and provides either a bipolar NRZ output or a NRZ output. The receive section accepts either a bipolar NRZ or a NRX input and provides baseband data and reconstructed clock outputs. The NRZ or the bipolar NRZ format for the transmit and receive sections are selectable with internally located modem switches.

b. Input Circuits. The input data is accepted through the standard digital inputs from local users. Input selection and circuit functions are described in detail in paragraph 2-3.

c. Transmit Bit Synchronizer/Clock Synthesizer. The purpose of the bit synchronizer is twofold; derive data clock (timing) for those data streams from the input circuits that do not have an accompanying clock signal, and to smooth any input phase jitter or bit distortion of the input signal. The clock synthesizer allows the transmit bit synchronizer to operate at any five digit input data rate from 19.200 kb/s to 5.0000 Mb/s. The bit sync/synthesizer form a phase lock loop that acquires the input data with rate offsets (actual rate compared to INPUT DATA RATE switch setting) of over 250 parts per million, and derives both bit rate and twice bit rate clock signals for use in the processing circuits. The phase lock loop also provides the phase jitter and data bit distortion smoothing. The clock input from the digital user can also be selected as the source for the bit synchronizer. An advantage of using the clock as an input is that it always has maximum transition density, providing the transmit bit synchronizer with the highest possible number of phase updates to the phase lock loop. The input data is then retimed by the smoothed clock signal, thus removing distortion from the input data. The bit synchronizer and clock synthesizer controls and circuit functions are described in detail in paragraphs 2-4 and 2-5.

d. Coders and Interface.

(1) The nature of some digital communications links results in an ambiguity between digital ONE's and ZERO's in the detected data stream. To eliminate this ambiguity, differential encoding of the input data is provided. In the differential coder, the standard Non-Return to Zero-Level (NRZ-L) code (the logic ONE/ZERO information is represented by different levels) is converted to an equivalent NRZ-M (mark) code (the logic ONE/ZERO information is represented by a transition or no transition). The differential decoder in the receive side reconverts the code to NRZ-L.

(2) An interface through high speed, current mode balanced line drivers and receivers is provided between the modem and an external error correcting coder. This permits selection of high gain coders when required. All encoding function may be bypassed completely if desired. The controls and circuit functions of the coders and interface are described in detail in paragraph 2-6.

e. Drivers. The driver outputs permit interfacing

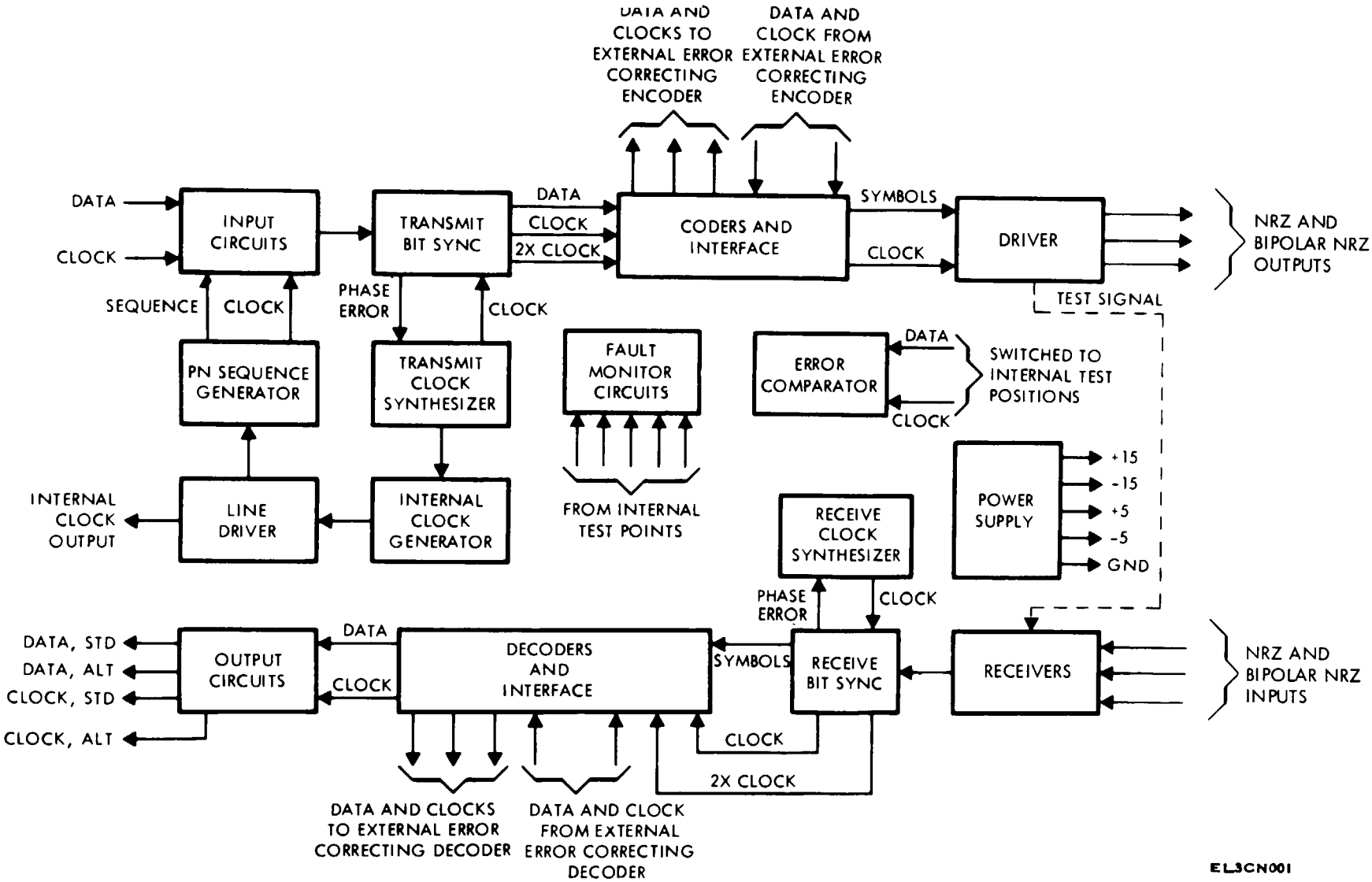

Figure 2-1. ICF modem, functional block diagram

the ICF Modem with a remotely located communications terminal. A LOS microwave link, a shielded cable, or a fiber-optic cable link can comprise the interconnect facility used for the interface. The LOS/ cable drive circuit converts the transmitted signal to a bipolar NRZ code format. A separate driver circuit is used to transmit the NRZ format output. The circuit functions are discussed in paragraph 2-7.

f. Receivers. The LOS/cable receiver/decoder circuit accepts a bipolar NRZ input signal from the interconnect facility, provides the appropriate gain and delay equalization, and reconverts the signal to a logic-compatible NRZ format. An additional receiver circuit is provided for accepting input NRZ signals from the interconnect facility. These circuit functions are discussed in paragraph 2-8.

g. Receive Bit Synchronizer/Receive Clock Synthesizer. The data bit decision and clock recovery functions are accomplished by the receive bit synchronizer and the receive clock synthesizer. The combination of these functional blocks forms a phase locked loop which regenerates the clock signals required for the signal processing circuits. The function of this phase locked loop is essentially the same as the Transmit Bit Synchronizer/Synthesizer described in c above. The unique details of the functions are discussed in paragraphs 2-9 and 2-10.

h. Decoders and Interface. The decoders and interface circuits reconstruct the original communications link input data. When error correction encoding has been performed at the other end of the link, an external decoder may be selected as required for processing the received signal. The built-in differential decoder is independently selectable. For uncoded inputs, all decoding functions may be bypassed completely. The details of the circuit functions and selection are provided in paragraph 2-11.

i. Output Circuits. The output circuits provide standard data and clock signals from the decoders and interface outputs to a local digital user. Identical alternate data and clock outputs are also furnished.

j. Internal Clock Generator. The transmit clock synthesizer provides signals which are used by the internal clock generator to provide a stable output clock to the digital user at the selected input data rate. These circuits are discussed in detail in paragraph 2-13.

k. Test and Monitor Circuits. Test and monitor circuits within the ICF modem allow monitoring of the operation of the link and provides a means of rapidly localizing malfunctions. Primary signals within the modem are monitored and their status is displayed on front panel lamps or a front panel meter. A pseudo-random sequence generator in the test circuits provides a known modulated signal at the output for link testing transmission. An error comparator in the receiver section detects and initiates a display of errors occurring in this pattern

as received from the communications link. For self-testing, a transmitter test output is relay coupled into the receiver, and the error comparator evaluates the pattern at various functional block outputs. These functions are discussed in paragraph 2-14.

2-3. Input Circuits.

a. General. The input circuits (fig. 2-2) receive standard clock and data inputs and a test sequence from the pseudo random (PN) sequence generator.

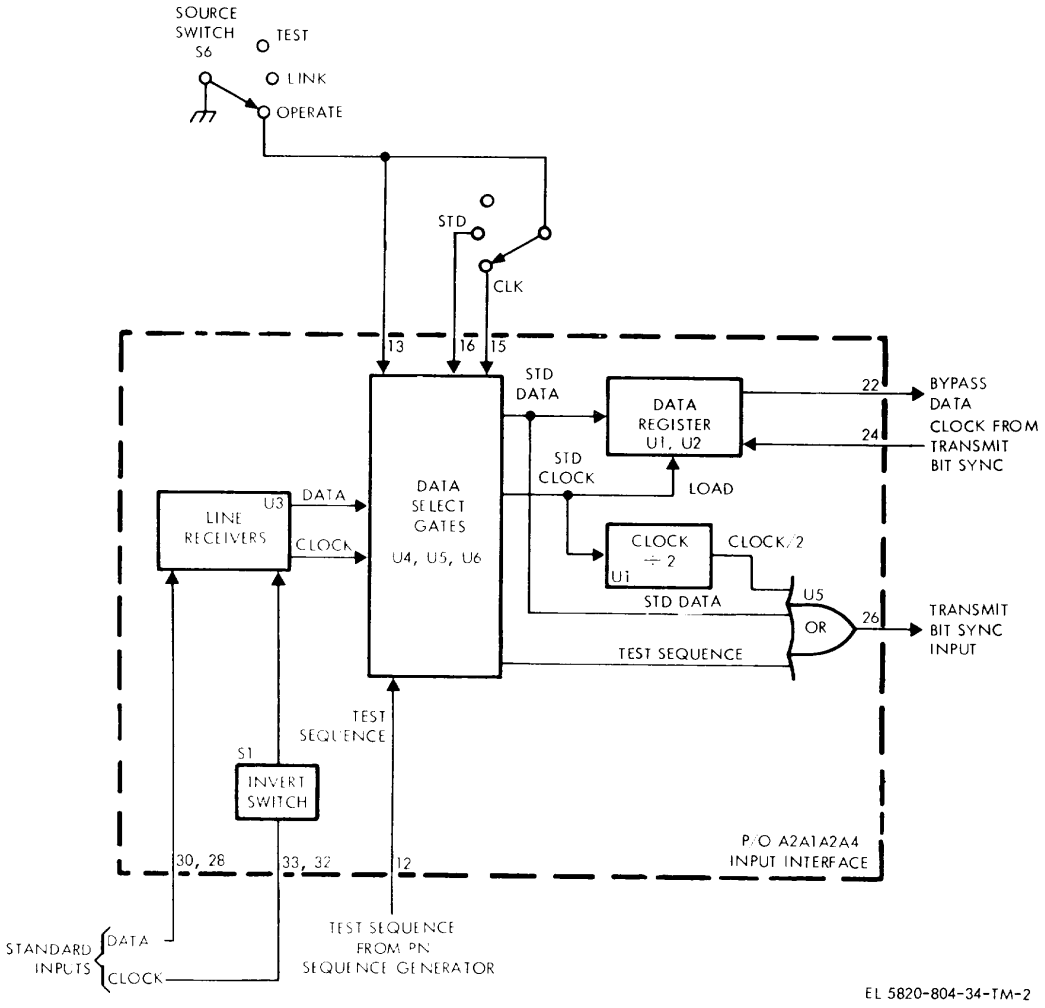

Figure 2-2. Input circuits, functional block diagram.

(1) With the STD/CLK/ICF switch set to STD, the standard data input is routed through the input line receivers, gated through the data select gates, and applied through the output OR gate to the transmit bit synchronizer.

(2) With the STD/CLK/ICF switch set to CLK, the standard data input is gated through the data select gates to the data register and loaded into the register by the standard clock input. Standard data is then transferred from the data register

directly to the coders and interface, bypassing the transmit bit synchronizer. To maintain synchronization, the accompanying standard clock is divided by two (to provide a signal with one transition during each bit period) and routed to the data input of the transmit bit synchronizer.

(3) When the SOURCE switch is set to the OPERATE position, the input data selection is controlled by the STD/CLK/ICF switch as indicated above. If the SOURCE switch is set to either the LINK or TEST position, the STD/CLK/ICF switch is disabled, and the test sequence from the PN sequence generator is routed to the transmit bit synchronizer input.

b. Input Interface (fig. FO-4). The input interface receives standard input data and clock from the digital user and test sequence data from the PN sequence generator. The type of data to be transmitted to the bit synchronizer is selected by inputs from the front panel STD/CLK/ICF switch and the transmit SOURCE switch.

(1) The standard input data, received via P1-30 and 28 is applied through one section of dual line receiver U3 to AND gate input U5-1 and to steer inputs 2 and 3 of flip-flop U1. If the STD/CLK/ICF switch is in the STD position and the SOURCE switch is in the OPERATE position, AND gate U5 pins 2, 4, and 5 are enabled by a ground input on P116 and standard data is gated through OR gate U5 (output pin 8) to provide the data input to the transmit bit synchronizer.

(2) Input standard clock is received through switch S1 (which permits clock in version) and applied through the second section of dual line receiver U3. If the STD/CLK/ICF switch is in the CLK position and the SOURCE switch is in the OPERATE position, the line receiver is enabled by a ground input on P1-15 to gate the clock to the trigger inputs of both flip-flops of U1. In this mode, standard data is loaded in flip-flop U1 (output pin 5) at the input clock rate and shifted to flip-flop U2 by the clock input from the frequency synthesizer. The output of U2 is then routed directly to the differential encoder. The clock divided by two output of U2-9 is OR'ed by U5 and used as the data input to the bit synchronizer.

(3) The test sequence input (P1-12) from the PN sequence generator is applied to pins 9 and 12 of AND gates of U6. When the SOURCE switch is in the OPERATE position, U6-8 is disabled by a ground input at P1-13. The test sequence is gated via OR gate U5 to the bit synchronizer when the transmit SOURCE switch is in the LINK or TEST positions. The STD/CLK/ICF switch is also disabled when the SOURCE switch is in the LINK or TEST positions, which disables the standard data and standard clock inputs. Refer to figure 2-2 for the switch connections.

2-4. Transmit Bit Synchronizer

a. General. The bit synchronizer (fig 2-3) provides a phase lock loop to maintain synchronization of transmitted bit rate and data. The input NRZ-L data is clocked into the bit detector phase flip-flop at beginning of bit period and into the data flip-flop at mid-bit period. Also at mid-bit period, the contents of the two flip-flops are transferred to the storage register. The transition detector compares the data from the storage register (preceeding data bit) with the content of the data flip-flop (present data bit) to determine whether a transition has occurred. An adder compares the stored phase bit with the present data bit. These bits are the same if bit rate is in sync or slightly behind data and the adder output is a ONE. If bit rate is ahead of data, the phase flip-flop loads the preceding bit and the adder output is a ZERO. Thus, the transmit bit detector acts as an early/late transition detector. If a transition has occurred, the adder output is gated to the loop filter. The DATA output of the data flip-flop is also applied to a retriggerable one-shot circuit. The circuit has a relatively long output pulse and is triggered by normal data transitions so frequently that its output is not allowed to expire. However, when data input ceases, the pulse expires and a loss of lock signal is routed via an OR gate to the alarm card. A second one-shot receives outputs from the loop filter up/down counter overflow circuits. Whenever the counter capacity is exceeded, the one-shot is triggered to develop a negative output to indicate loss of lock.

The loop filter arithmetic circuits receive the phase MSB and transition bit (the MSB is jumpered to three loop filter inputs). These bits are added to bits previously received to develop an up or down count to the accumulator. The accumulator is equipped with overflow detection circuits that provide input to the loss of lock circuits on the transmit bit detector. The accumulator output is added to the contents of the input register to develop an 8-bit digital control word representing phase error. The adder output is then loaded into a storage register on the D/A converter card. The output of the D/A input register is converted to an analog current by the D/A converter. The analog current is used as a phase correction signal to the transmit frequency synthesizer.

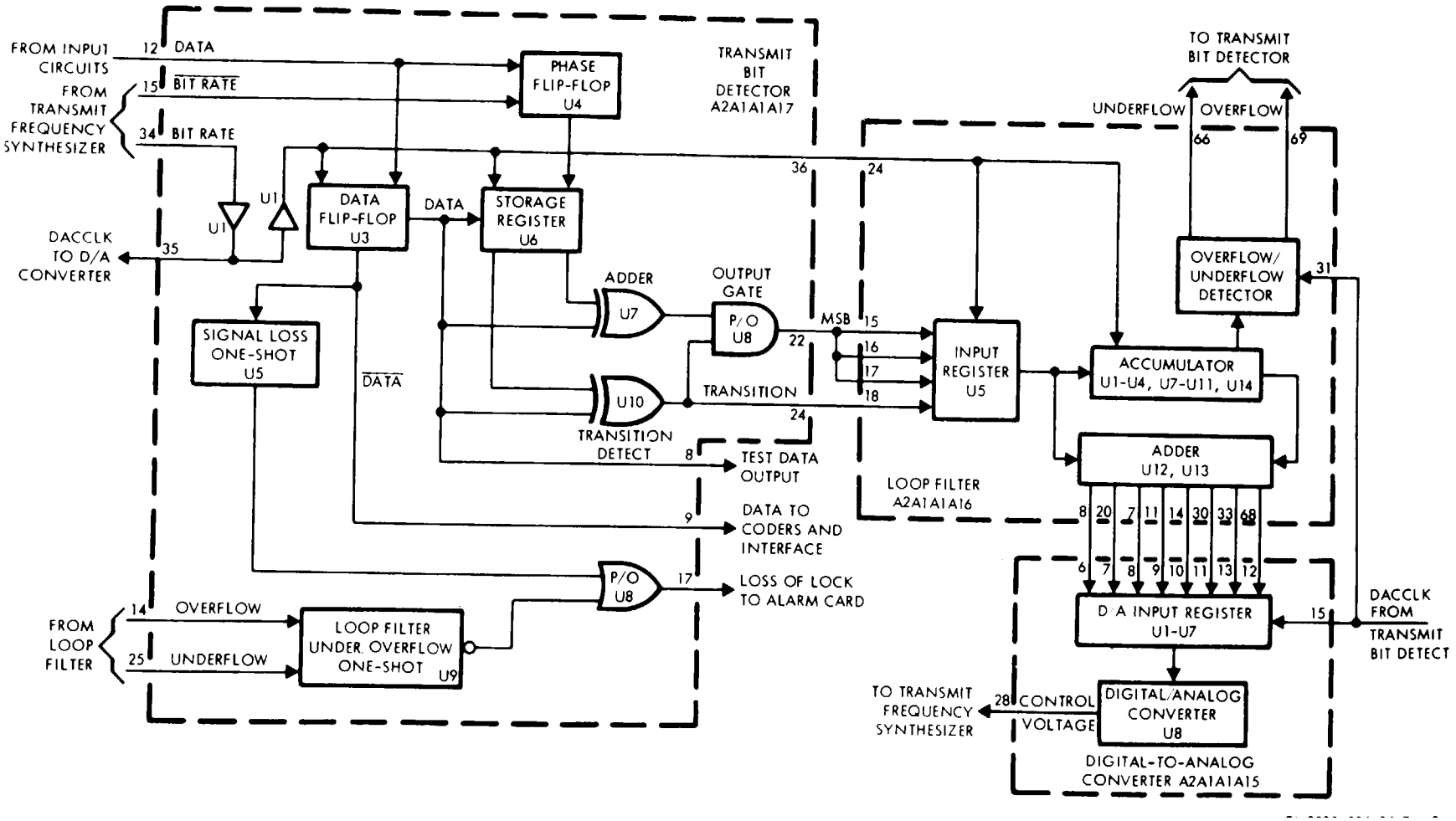

Figure 2-3. Transmit bit synchronizer, functional block diagram.

b. Transmit Bit Detector (fig. FO-5). The transmit bit detector receives data and bit rate inputs and provides outputs to the loop filter indicating whether bit rate leads or lags the data. The transmit bit detector also provides a loss of lock indication when data stops or when the loop filter up/down counter overflows (in either direction).

(1) The transmit data input (P1-12) is applied so pin 2 of data flip-flop U3 and pin 2 of phase flip-flop U4 (the other flip-flops of U3 and U4 are not used). The bit rate complement (P1-15) is delayed by double inversion through circuits of U2 and loads data into phase flip-flop U4. If clock and data are exactly in sync or if clock lags data, phase flip-flop U4 is loaded near the leading edge of data. If clock leads data, the flip-flop is loaded near the trailing edge of data. The Q output of U4 is applied to the C input of storage register U6.

(2) Bit rate true (P1-34) is received through circuits of U1 and, at mid-bit period, clocks storage register U6 to load the contents of phase flip-flop U4 into the C stage and to load the previous data bit from data flip-flop U3 into the A stage. Bit rate true also loads the new data bit into data flip-flop U3. (Refer to figure 2-4 for bit detector timing.)

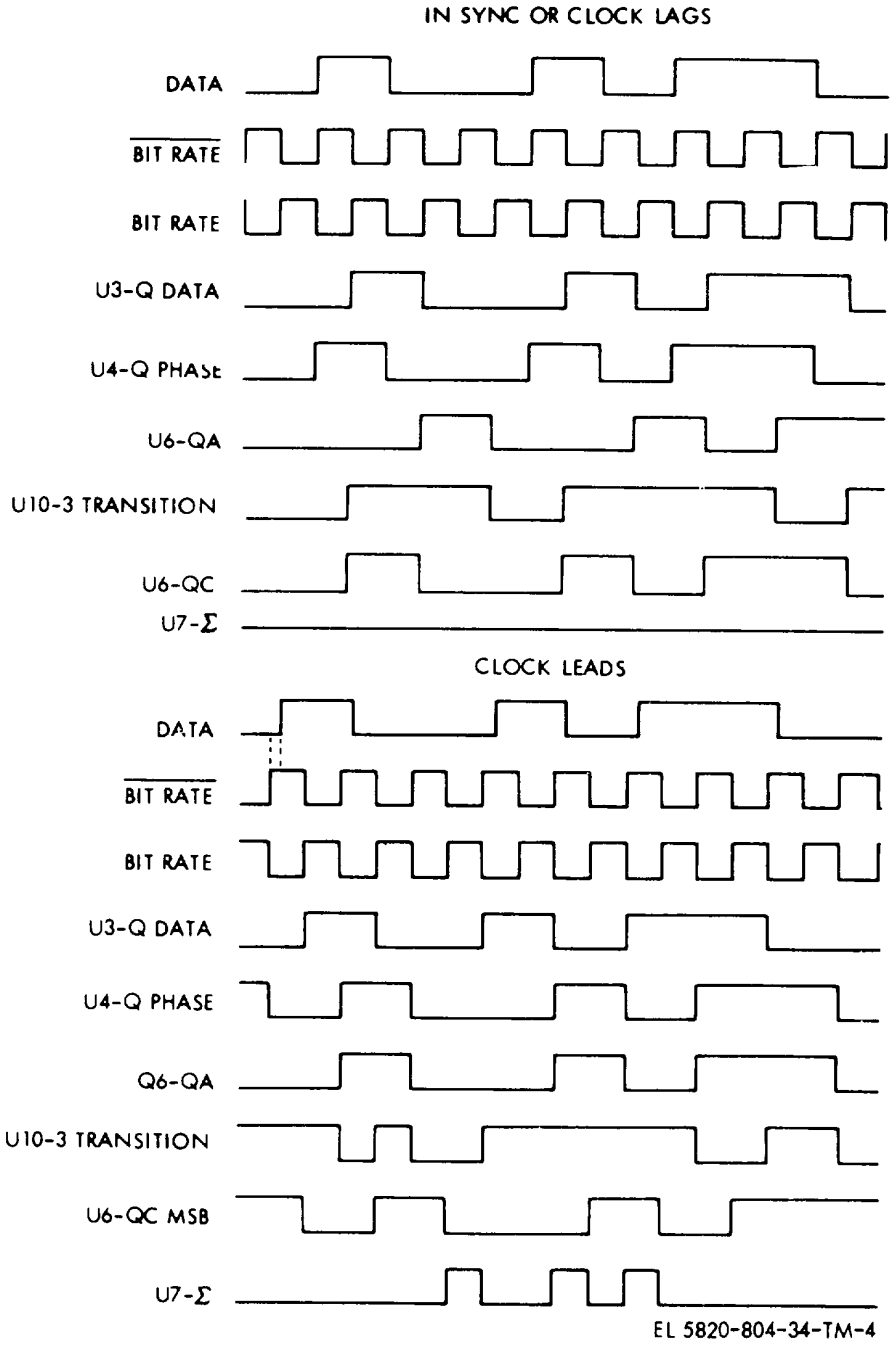

Figure 2-4. Transmit bit detector, timing diagram.

(3) Exclusive OR U10 compares the new data bit from the Q output of U3 with the previous data bit from the QA output of storage register U6 to determine whether a data transition has occurred. The data transition signal enables gate U8 and is routed to the loop filter via P1-24. detector, timing diagram.

(4) The MSB input to the loop filter is formed by adder U7. This circuit sums the output of data flip-flop U3 and the output from Q c of storage register U6 (with a constant ONE carry input). Since the data flip-flop and storage register are clocked simultaneously, the adder inputs will be the same if the phase flip-flop loaded

the current data bit (clock in sync with the data or clock lagging data). With both inputs the same, the adder output is a ONE.. Assuming a data transition and clock leading data, the phase flip-flop would load the previous data bit, the adder inputs would differ, and the adder output is a ZERO. The adder output is AND'ed with the transition bit and the resultant output MSB (U8-12) s routed to the loop filter via P1-22.

(5) Circuit U5 is a retriggerable one-shot with an output pulse period exceeding six seconds. The one-shot is triggered each time a data ZERO is loaded into flip-flop U3, thus maintaining a high to pin 3 of U8. If data ceases, the one-shot output expires and a loss of lock indication (logic ZERO) is developed by gate U8 at P1-17.

(6) Loss of lock is also developed when the loop filter up/down counter overflows. Either an under or an over count signal from the loop filter triggers one-shot U9. The negation output of the one-shot, via U8, then provides a loss of lock signal to the alarm card.

(7) The bit detector also provides true and complement clock and data outputs. Bit rate complement from U1-6 is routed to the loop filter, the D/A converter, and to the self-test circuits. Bit rate from U1-8 is routed to the loop filter and D/A converter. Data complement from U3-6 is routed to the coder switch and data true from U3-5 is routed to the self-test circuits.

c. Loop Filter (fig. FO-6). The loop filter receives four input bits developed from the phase error decision and the transition signal, and bit rate timing inputs. The circuit provides the digital equivalent of a lead integrate analog filter and its output is an eight bit word to the D/A converter.

(1) Figure 2-5 illustrates the loop filter function. The four bit word representing the phase error input is loaded into an input register. An arithmetic unit accumulates the successive phase words by adding each phase word input to the number stored in the arithmetic unit. An 8-stage up/down counter increases the accumulator capacity. The counter is incremented up or down each time the capacity of the arithmetic unit is exceeded. The final output to the D/A converter is developed by adding the input word to the accumulator output. The output, therefore, is a function of two factors; the phase word in the input register, and the cumulative result of previous phase words.

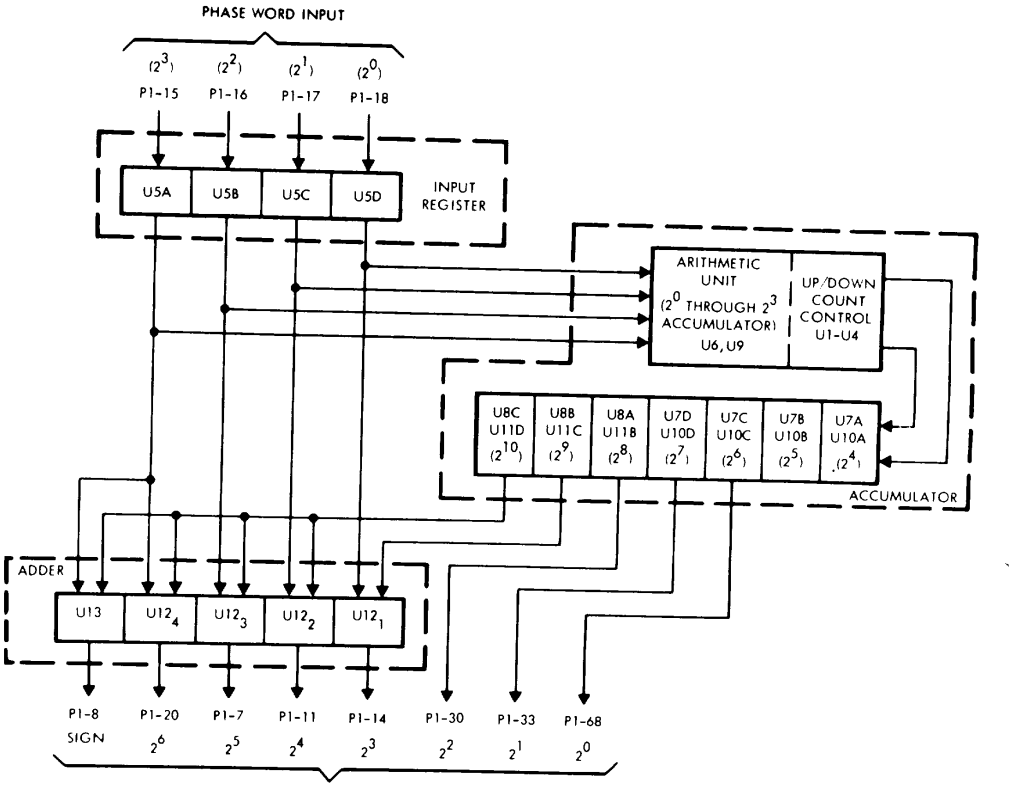

Figure 2-5. Loop filter, functional block diagram.

(2) The phase word, which is developed from the phase error decision and the transition signal, is loaded into the input register by bit rate clock applied to P1-24. The format of the phase word is defined in table 2-1. When no transition has occurred, the phase word input is all ZERO's. When a transition occurs, the phase word represents a weight and magnitude associated with the detected phase error. In the transmit bit synchronizer, P1-16, P1-17, and P1-18 are connected together in the card file; thus the input phase word associated with each transition is either a + 1 or -1 depending on the early/late gate operation of the transmit bit detector.

Table 2-1. Phase Work Format

Phase error input	P1-15 (2^3)	P1-16 (2^2)	P1-17 (2^2)	P1-18 (2^0)
+7	0	1	1	1
+5	0	1	0	1
+3	0	0	1	1
+1	0	0	0	1
-1	0	0	0	0
-3	1	1	0	1
-5	1	0	1	1
-7	1	0	0	1

(3) Adder circuit U6 adds each new phase word with the sum of the previous associated words circulated through register U9. As an example of adder operation, assume U9 contains a binary 9 (1001) and a phase word representing +3 (0011) is present in the input register. The result at the sum output of U6 is a binary 12 (1100), which is entered into U9 at the end of the clock period. The next phase word will be entered into the input register U5 and simultaneously added to the contents of U9 during the next clock period. Assuming this next phase word is a -5, the result at the sum output of U6 will then be;

$$\begin{array}{r} 1100 \\ +\ 1011 \\ \hline (1)0111 \end{array}$$

where the parenthetical 1 represents a carry output. The 4-bit sum output of U6 is a binary 7, which is 5 less than the previous number. In the case where the input phase word represents no transition (0000), the sum output of U6 is identical to the contents of U9, and the output of U9 does not change.

(4) Up/down count control to the balance of the accumulator circuitry is controlled by U1-U4. As shown in table 2-1, the LSB (P1-18) of the phase word input is a transition/no transition indicator and the MSB (P1-15) is a sign indicator. When a positive phase word is present in input registerd U5 (QA low and QD high), the up count control is generated if a carry output from U6 is present. U6-14 high will result in a low at U2-6, and an up count control pulse will be developed at U4-11 afterd U3-6 goes high on the next clock pulse. When a negative phase work is present in input register U5 (QA and QD high), the down count control is developed at U4-8 if no carry output is developed by U6 (U6-14 low).

(5) Since the binary counter chain of U7 and U8 upcounts once each time an overflow from U6 occurs and downcounts each time an underflow occurs, each successive counter stage contains an increasingly significant bit in a binary number representing the phase work accumulation. The status of counters U7 and U8 are transferred into storage registers U10 and U 11 at the end of each clock period.

(6) The outputs of the phase word accumulator beginning with the bit representing 26 are used to provide the less significant bits to the D/A converter. The two most significant bits of the phase accumulation are added to the input register by adder U12 with the input bit representing 20 weight being used to develop the 23 input to the D/A converter. The magnitude of each D/A converter input word is therefore equivalent to:

(Input register state x 8) + (Phase word accumulation + 64)

The sign bit to the D/A converter is developed by adder U13.

d. Digital to Analog Converter (fig. FO-7). The digital to analog (D/A) converter accepts the 8-bit output of the loop filter and develops an equivalent analog output to control the frequency of the frequency synthesizer. The 8-bit output of the loop filter is applied to steer inputs of flip-flops U1 through U4. These flip-flops are loaded at bit rate and their outputs drive the D/A converter. The D/A output provides a current source (maximum +.5 milliamperes) to control the frequency of the synthesizer.

2-5. Frequency Synthesizer

a. General. The frequency synthesizer (figure 26) functions as the voltage controlled oscillator for the bit synchronizer. The effective VCO center frequency is selected by five front panel digit switches while tuning is accomplished by the control input from the bit synchronizer. The synthesizer operates over the center frequency range of 10 kHz to 9.9999 MHz, while the tuning range available to the bit synchronizer is a minimum of +0.025 percent of the selected bit rate. The frequency synthesizer utilizes an indirect phase lock loop to develop a stable programmable reference frequency that is then mixed with the output of a VCO. The VCO is tuned by a control input from the bit synchronizer. The difference frequency output between the programmable reference and the VCO is downcounted to produce the center frequency selected by front panel switches.

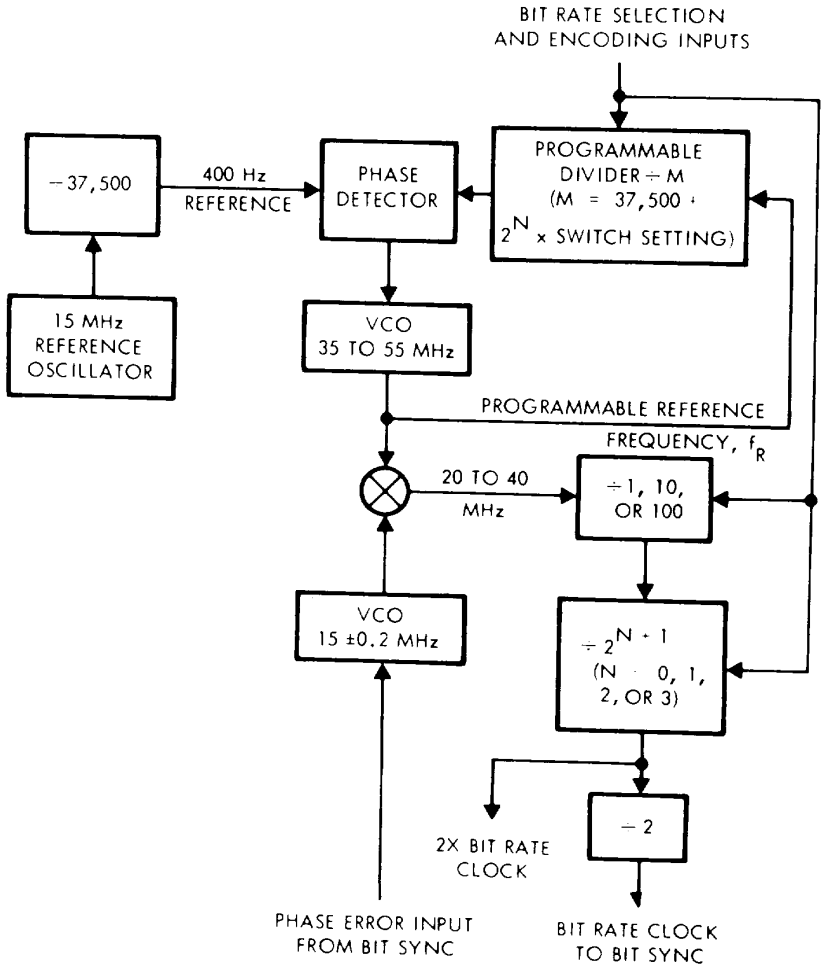

Figure 2-6. Frequency synthesizer general block diagram.

(1) The synthesizer reference frequencies are developed from a 15 MHz temperature compensated crystal oscillator (TCXO). The output of this oscillator is divided by 37,500 by the reference divider to develop a 400 Hz reference signal to the phase detector.

(2) The phase detector produces a voltage output proportional to the phase difference between the 400 Hz reference signal and the programmable divider output signal. This voltage is then applied to the VCO to adjust the output frequency between 35 and 55 MHz. The VCO output frequency is applied back to the programmable divider input.

(3) The programmable divider divides the VCO output by a number, M, which varies between 87,500 and 137,499 depending on the encoded bit rate selection control inputs. Since the programmable divider output is applied back to the phase detector input, a feedback loop exists which adjust the VCO to maintain a 400 Hz programmable divider output. Therefore, the VCO provides an internal programmable reference frequency, f_R, at a rate equal to 400 Hz x M, where M is the selected division ratio of the programmable divider.

(4) The final output frequency is derived by mixing the programmable reference frequency with the output of the 15 MHz VCO, which is controlled by the bit synchronizer. The resultant difference frequency is then divided by selectable decade and binary counters to produce a nominal output rate equal to selected data rate; however, the exact output rate is dependent on the 15 MHz VCO output.

(5) The output frequency is controlled by using the digital thumbwheel switch settings, a number, N, which is derived from the digital thumbwheel switch settings, and the decade switch setting to control the various internal frequency dividers. Operation over the full output frequency range is accomplished by operating in three decade ranges, as indicated on the thumbwheel decade selection switch, and by internally subdividing each decade range into four octave ranges. The octave range of operation defines the value of N as indicated in table 2-2.

Table 2-2. Synthesizer Range Selection

Range	Digital thumbwheel switch setting	N.
A	10000 to 12499	3
B	12500 to 24999	2
C	25000 to 49999	1
D	50000 to 99999	0

(6) To illustrate the frequency synthesis process, assume a case in which an input data rate of 170.00 kb/s has been selected. It can be seen from table 2-2 that the digital thumbwheel switch settings will cause the synthesizer to operate in range B (N = 2). The programmable divider ratio, M, is given by the expression :

$$M = 37{,}500 + (2N \times \text{switch setting})$$

therefore:

$$M = 37{,}500 + (4 \times 17{,}000) = 105{,}500$$

Since the internal phase locked loop forces the programmable reference frequency, f R, to be equal to 400 x M, then:

$$f_R = 400 \times 105{,}500 = 42{,}200{,}000 \text{ Hz}$$

The center frequency input to the decade divider is obtained by subtracting 15 MHz from f_R, which yields a center frequency of 27,200,00 Hz. The divide by 10 function is selected in this case, and the decade counter produces an output of 2,720,000 Hz. Since N is 2, the 2 N + 1 counter output is 2,720,000 Hz + 8, or 34,000 Hz. This signal is available as the 2 x bit rate clock. The final + 2 stage produces a bit rate clock at 170,000 Hz, which is equal to the INPUT DATA RATE switch setting of 170.00 kb/s.

(7) Internal operating rates and ratios for various INPUT DATA RATE switch settings between 1.0000 and 9.9999 Mb/s are given in table 23. For the switch settings shown, the decade divider is programmed to divide by 1. Operation in the lower decade range is identical except that the decade divider is programmed to divide by 10 or 100 as required.

Table 2-3. Divider Ratios and VCO Outputs

Range	Switch setting	Multiplier	Constant	Divider ratio	VCO output (MHz)	VCO -I5 MHz	N +1 2	2Rout (MHz)	Rout (MHz)
D	99999 x	1	+37500	= 137499	54.999600	39.999600÷	2	19.999800	9.999900
(N = O)	50000 x	1	+ 37500	= 87500	35.000000	20.000000 ÷	2	10.000000	5.000000
C	49999 x	2	+ 37500	= 137498	54.999200	39.999200 ÷	4	9.999800	4.999900
(N=1)	25000 x	2	+ 37500	= 87500	35.000000	20.000000 ÷	4	5.000000	2.500000
B	24999 x	4	+ 37500	= 137496	54.998400	39.998400 ÷	8	4.9998000	2.499900
(N=2)	12500 x	4	+ 37500	= 87500	35.000000	20.000000 ÷	8	2.5000000	1.250000
A	12499 x	8	+ 37500	= 137492	54.996800	39.996800 ÷	16	2.499800	1.249900
(N=3)	10000 x	8	+ 36500	= 117500	47.000000	32.000000 ÷	16	2.000000	1.000000

b. Description.

(1) The output of the 15 MHz reference oscillator (fig. 2-7) is applied to a power divider, which provides an output to the internal clock generator and drives a level converter. The converted 15 MHz signal is applied to a fixed counter on the reference divider card. The counter divides by a ratio of 37,500 to produce a 400 Hz reference pulse to the phase detector.

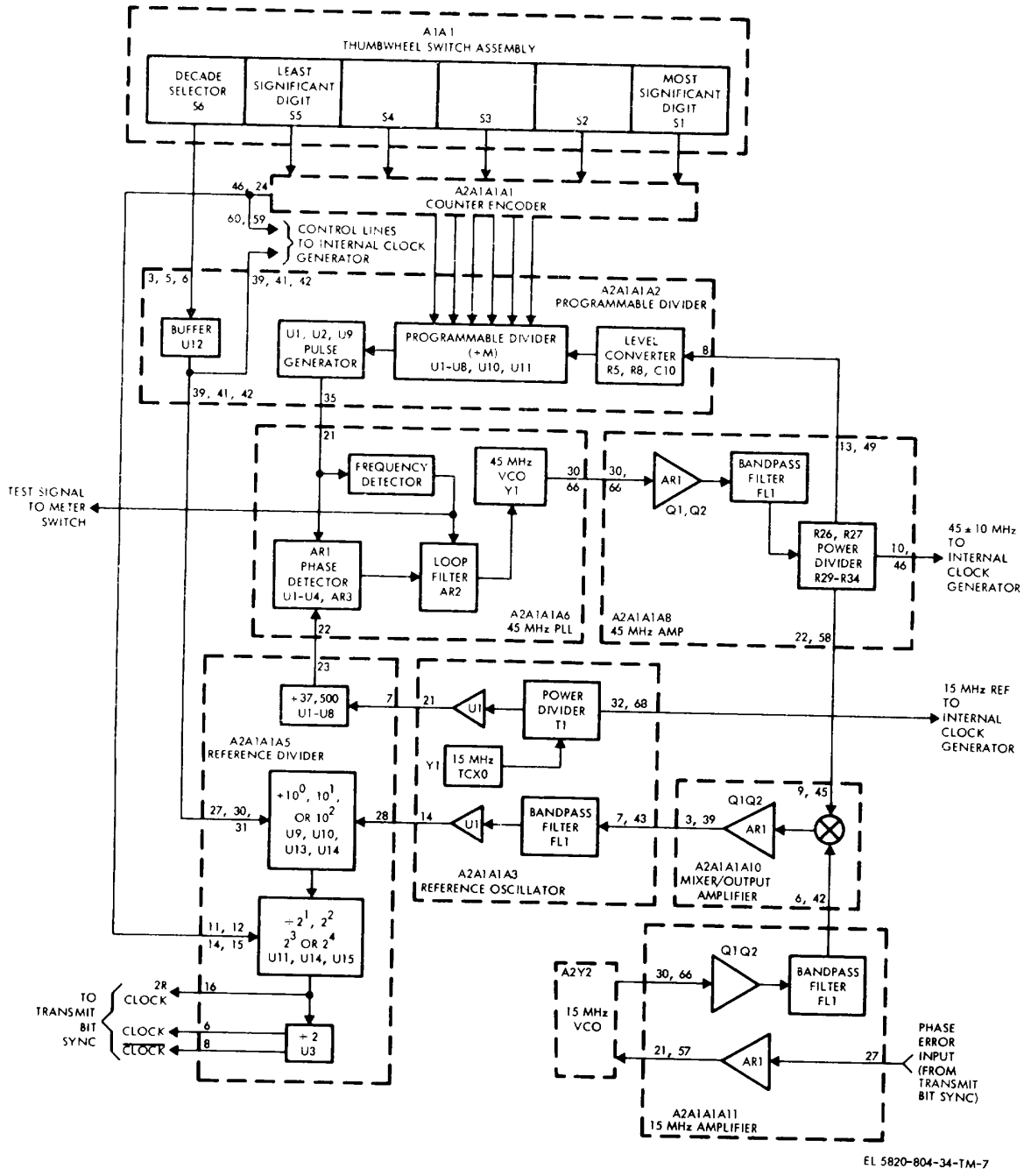

Figure 2-7. Transmit frequency synthesizer, functional block diagram.

(2) The phase detector uses the 400 Hz reference signal to produce an internal voltage ramp each time a reference pulse is received. The output pulse from the programmable divider is then used to sample the ramp voltage. The resultant phase detector output is a voltage proportional to the chase difference between the reference pulse and the Programmable divider output. When the loop is locked, this voltage is used to control the 45 MHz VCO via the loop filter. For acquisition, a frequency detector generates a voltage proportional to the difference between 400 Hz and the output rate of the programmable divider. This voltage is added to the loop filter input, and is also used as a test output.

(3) The 45 MHz VCO output is amplified and filtered on the 45 MHz amplifier card, and distributed to the internal clock generator, the mixer, and the programmable divider input via a power divider.

(4) The programmable divider counts down the VCO output to maintain operation of the phase lock loop at 400 Hz. This is accomplished by first dividing the VCO output by the constant 37,500 plus 1, 2, 4, or 8 times the bit rate switch setting, dependent upon the selected bit rate octave. The 400 Hz output pulse from the programmable divider closes the phase lock loop.

(5) The counter encoder decodes the digital thumbwheel switch settings to determine the octave range of operation and control the number of times the programmable divider divides by the thumbwheel switch setting. The decoder octave range output is also provided to the internal clock generator and the programmable binary counter. The counter encoder also provides the constant 37,500 input to the programmable divider.

(6) The control input from the bit synchronizer is applied through a current-to-voltage amplifier to 15 +0.2 MHz VCO. The 15 _0.2 MHz VCO output is amplified, filtered, and applied to the mixer/output amplifier. The difference frequency output from the mixer, ranging from 20 to 40 MHz, is routed through a low pass filter to a divider chain. A decade divider is included to provide -1, + 10, and 100 functions. The 1 function is used for all bit rates over 1.0000 MHz. The -10 and +100 functions provide decade division for frequencies below 1.0000 MHz. Following the decade counter, a binary counter provides division ratios of 2, 4, 8, 16, ,s selected by the counter encoder, to produce twice the desired bit rate. The output stage is a divide by two flip-flop which provides the bit rate output.

c. Reference Oscillator (fig. Fo-8). The reference oscillator card contains the 15 MHz temperature compensated crystal oscillator (TCXO) and a 30 MHz band-pass filter. Also included on this card is a power divider and level converters.

(1) The reference frequency for the synthesizer is developed by 15 MHz TCXO Y1. This oscillator is stable within -2 ppm/3 months. The oscillator output is transformer-coupled to one half of dual high speed ECL to TTL level converter U1. The output of U 1 is compatible with the divide by 37,500 circuit on the reference divider.

(2) Bandpass filter FL1 receives the 20-to 40 MHz output of the mixer/amplifier card through a 3 dB attenuator (R3, R5, and R6). The filter center frequency is at 30 MHz, the 1 dB bandwidth is 20 MHz, and the 15 dB bandwidth is 30 MHz. The 30 dB bandwidth is 40 MHz. The output of FL1 is applied through a resistive power divider to the other half of ECL to TTL level converter U1. The level converter output then drives the selectable decade and binary dividers on the reference divider card and the other power divider output (P1-32, 68) is available to the internal clock generator circuit.

d. Reference divider (fig. FO-9). The reference divider provides a divide by 37,500 countdown of the output of the 15 MHz TCXO to produce 400 Hz reference pulses to the phase lock loop. The reference divider card also contains a decade counter to divide the 20-40 MHz output of the mixer/amplifier by 1, 10, or 100 dependent upon front panel decade rate range selected. The decade counter output is then applied to a straight binary counter that further divides the clock signal by 2, 4, 8, or 16 (2N 1) depending on outputs from the counter encoder. The output of the binary counter is 2 times bit rate which is further divided by two to produce bit rate.

(1) The level converted 15 MHz output of the temperature compensated crystal oscillator (TCXO) is divided by a J-K flip-flop of U3 (P1-7) to develop 7.5 MHz into binary counters U4 and U5. Counters U4 and U5 are short counted to divide by 75 (rather than 256) by utilizing the load inputs to preset a count of 181 each time a carry output from U5 occurs. The 100 kHz is used to clock the divide by five counter U6, divide by 50 counters U7 and U8, and output flip-flop U12.

(2) The divide by five counter U6 is preset to count six and the output count 10 is detected by U2 to again preset the counter and to enable divide by 50 counters U7 and U8. These counters are short-counted by presetting to count 206 using the carry output of U8 and the decoded count 10 output of U6 (U2-3) via U2-11. The 400 Hz carry output of U8 steers flip-flop U12 high and then low at a 400 Hz rate to produce a 400 Hz, 50-microsecond positive pulse from the flip-flop (P1-23).

(3) Control for decade counters U9 and U10 is developed from the bit rate select range switch via inverters in the programmable divider. When no decimal division is required, U13-13 is enabled by the .-1 control signal (high on P1-30) and clock is routed directly through U13 and U14 to binary counter U11. The 10 control signal (high on P130) enables U13-9 to select the Q D output of U9 to the binary counter, and the -100 control signal (high on P1-21) enables U13-2 to select the QD output of U10 to the binary Counter.

(4) The counter encoder provides a four bit word to enable one of the U15 AND gates depending on the digital thumbwheel switch settings. These gates receive the 2, -4, +-8, and +-16 outputs of binary counter Ull11 and gate the selected output which is equal to selected rate times two. Bit rate times two (U14-6) is divided by a flip-flop of U3 to develop the bit rate output.

e. 45 MHz Phase Lock Loop (fig. FO-10). The 45 MHz phase lock loop card contains a phase detector, a loop filter, a 35-55 MHz VCO, and a frequency discriminator. The synthesizer phase locked loop is closed through the programmable divider card, where the VCO output is counted down to 400 Hz.

(1) The phase detector section of the phase lock is formed by analog switch U1, amplifier AR1, and analog gate U4. This section uses the hold-sample hold technique to develop the phase error voltage.

AR1 and C1 form an inverting integrator circuit. The maximum negative output voltage is determined by VR1 and CR1, which acts as a clamp at -6.2 volts. The integrator receives input currents from one of two sources:

(a) A positive inpur current from the + 15 volt supply via R2 and gate U1.

(b) A negative input current from the --15 volt supply via R1 and gate U1. At the beginning of the reference period, the positive reference pulse applied to P1-22 closes three parallel connected gate sections of U 1 and allows current to flow through R2 to the integrator. At this time the remaining gate section of U1 is also closed (fig. 2-8), but the current through R2 is much greater than the current through R1. Therefore, the integrator output goes negative until the -6.2 volt clamp voltage is reached. The three parallel-connected gate sections of U1 are opened at the end of the reference pulse and the integrator voltage begins a positive ramp due to the input current from R1. The output pulse from the programmable divider is applied to P1-21. When this negative-going pulse arrives, the output of U2-2 opens the U1 gate section connected to R1. The integrator receives no input current, and the integrator output voltage remains constant while the programmable divider output pulse is present. Since this pulse is also applied to P1-23, an internal analog gate in U4 is simultaneously closed. This allows the integrator output voltage to be transferred to C5, which acts as a storage element. The voltage on C5 is buffered internally by U4 and the buffered voltage appears on U4-11. At the end of the output pulse from the programmable divider, U1-3 is closed, the internal gate in U4 is opened, and the integrator output ramp continues until the next reference pulse arrives. If the loop is operating in sync with the reference pulse and the required VCO output frequency is 45 MHz, the hold signal would occur at mid-bit period as the integrator output is crossing through the zero volt level. A positive or negative output of U4 provides speed up or slow down control to the 45 +10 MHz VCO via the loop filter, AR2.

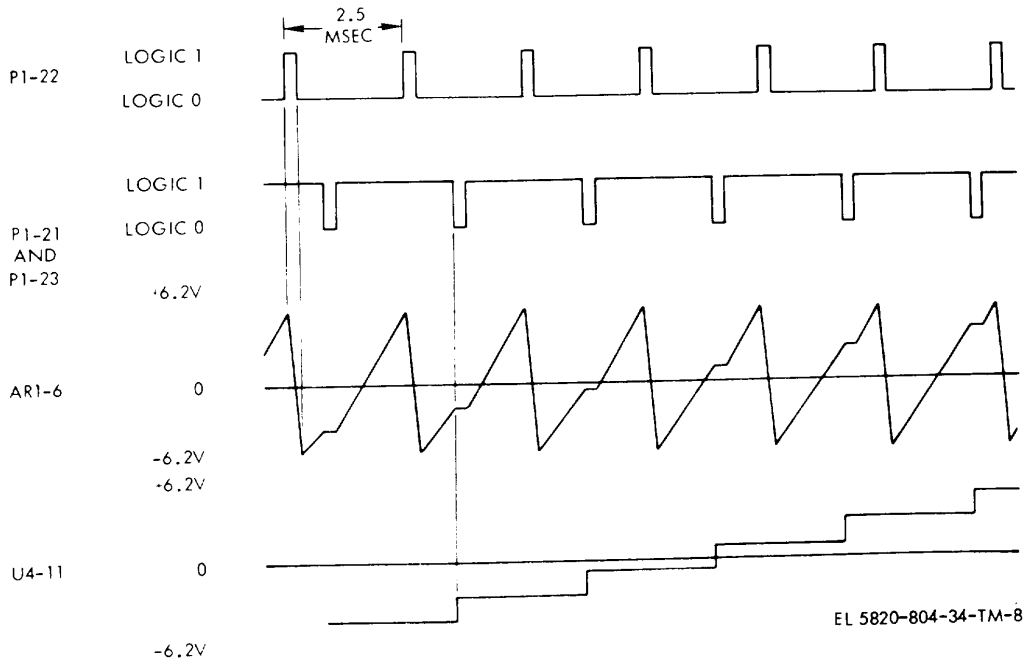

Figure 2-8. Synthesizer phase detector, timing diagram

(2) Amplifier AR2 and associated components form the loop filter at the input to the 45-10 MHz oscillator. The amplifier has a dc gain of approximately 80. A positive 10 volt output of the amplifier will drive oscillator Y1 to operate at 35 MHz, while a negative 10 volt output causes the oscillator to operate at 55 MHz.

(3) The frequency discriminator is formed by one-shot U3 and operational amplifier AR3. The one shot circuit is triggered by the trailing edge of each sample pulse and develops an output that is adjusted to one-half reference bit period in duration (1.25 milliseconds). When the phase lock loop is operating at 400 Hz, the average output of amplifier AR3 to the loop filter, which represents the sum of the currents through R20 and R15, is zero. When the loop is off-frequency, (not phase locked) the output AR3 to the loop filter provides an error voltage via ,e loop filter AR2 to correct the oscillator output. Resistors R18 and R21 condition the AR3 output to be compatible with the front panel meter.

f. 45 MHz Amplifier (fig. FO-11). The 45 MHz amplifier consists of three amplifier stages followed by a low pass filter. The amplifier input from the 45 +10 MHz VCO is amplified, filtered, and routed to the programmable divider, the mixer/output amplifier, and the internal clock generator. The 35 to 55 MHz output of the phase lock loop card, which is received at approximately -8 dBm, is further attenuated by 20 dB across resistors R5 through R7 and applied to the RF amplifier stages. The RF amplifier stages are formed by operational amplifier A R1 and transistors Q1 and Q2. The amplifier has an overall gain of approximately 40 to 45 dB as controlled by variable resistor R24. The amplifier bandwidth is 70 MHz. Each stage of the amplifier is transformer coupled to the next, and the output of transformer T2 is applied to 55 MHz low pass filter Fl,1. Filter FI.1 suppresses harmonics of the signal and provides an output that is attenuated, split, and routed to the mixer/output amplifier and the programmable divider.

g. Programmable Divider (fig. FO-12). The programmable divider functions within the phase lock loop to count down the 35 to 55 MHz output of the 45 +10 MHz VCO to provide 400 Hz sample pulses to, the sample and hold circuits. This is accomplished by first dividing the VCO output frequency by a 37,500 constant, then further dividing by the digital INPUT DATA RATE switch

setting multiplied by 1, 2, 4 or 8. The divider ratio is thus 37,500 + (2N x switch setting) as illustrated in figure 2-9.

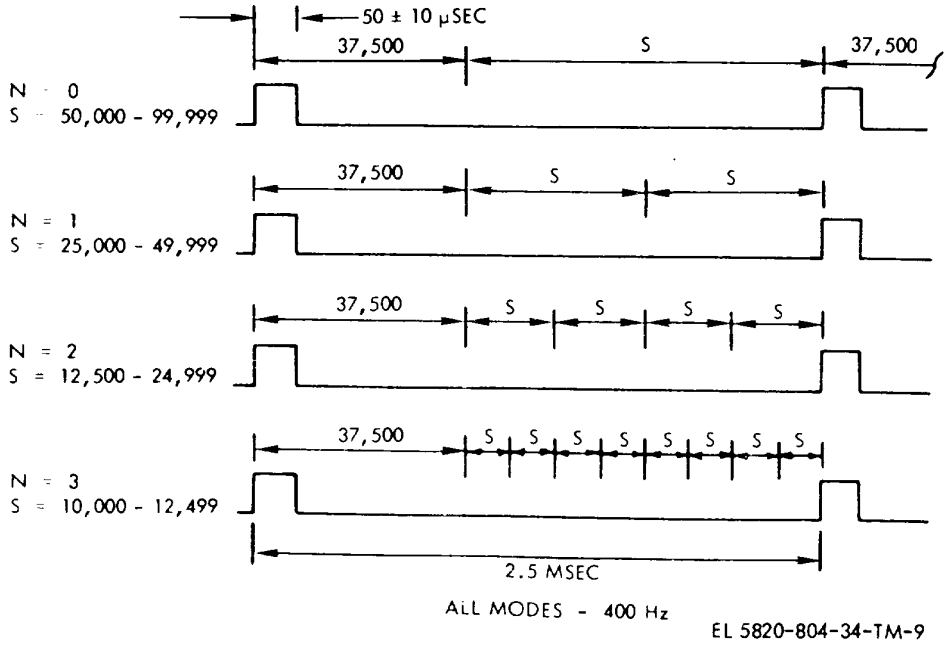

Figure 2-9. Counter divide by 37,500 + 2^Nx switch setting(s) modes

(1) The decade counters used in this application count clock pulses in a normal binary sequence up to a count of 9 (1001) which generates a carry output. The next clock pulse causes the counter to increment to 0 (0000), and the counting sequence is repeated. To achieve a specific count, the counter may be preloaded with the 9's complement code for the desired number (see table 2-4). For example, if a count of 6 is desired, the counter is preloaded with the 9's complement of 6, which is a binary 3 (0011). Then, six clock pulses will cause the decade counter to increment to a count of 9, causing a carry output.

Table 2-4. Thumbwheel Switch Coding

Switch setting	9's complement coding
0	1001
1	1000
2	0111
3	0110
4	0101
5	0100
6	0011
7	0010
8	0001
9	0000

(2) Counters U3 through U7 are decade counters that correspond to the least significant digit through the most significant digit, respectively. The counter array receives either the 9's complement of the fixed program constant of 37,500 (which is 62499) or the 9's complement output of the INPUT DATA RATE thumbwheel switches via the counter encoder. Counter U8 receives the output of the counter encoder that determines the multiplier; i.e., the number of times the switch selection shall be multiplied. By using 9's complementing, the counter array is preset to the value that will cause the desired number of clock pulses to result in a counter overflow.

(3) Because of the high clock rate, prescaling is required. Prescaler U11 divides by either 10 or 11 depending on whether Ull-3 is high or low, respectively. Counter U3 is loaded with the least significant digit and controls the counting of U11 Prescaler U11 repeatedly counts to 11 until U3 provides a carry out, after which U3 disables itself using the carry output via U1, and U11 provides a divide by 10 function. Transistor Q1 provides the ECL to TTL interface.

(4) To determine how the counter array increments the required number of times for each programmed input, assume a count of 12340 is desired. The 9's complement code for this number is equivalent to a BCD 87659, which would be the initial state loaded into U3 through U7. Since U3 in his case is preset to a count of 9, the carry output J3-15) would be high, forcing U11 to function simply as a 10 counter. The output rate from U11 is used to clock the rest of the counters, U4 through U7. U2 is connected to decode a load enable signal to the counters when a count of 8 is reached in U4, and U5 through U7 have all reached a count of 9. At this time, the total number of times that the -' 10 output of U 11 has occurred is 9998 8765 (the original state of U4 through U7), or 1233 times, and the total number of input pulses has been 1233 x 10, or 12330 input pulses. Since the load input is now enabled, the counter array will reload on the next output transition from U11, or after 10 more input pulses have been received. Therefore, the total number of input pulses occurring from the time the counter array is originally preloaded to the time the next preload occurs is 12330 + 10, or the desired count of 12340. If the desired count had been 12345, counters U4 through U7 would have functioned in the same manner. However, U3 would have been preloaded to count of 4 (9's complement of 5), and U11 would nave been forced to act as a I1 counter 5 times before reverting to a 10 counter. Therefore, five extra input pulses would have occurred during the process and the total count would have been 12340 + 5, or the desired count of 12345.

(5) The overall timing of the programmable divider is illustrated in figure 2-10 for a switch setting of 15430. At the end of the 37,500 count, flip-flop IJ9-6 is low, forcing U10-8 high which causes the counter encoder to present the switch setting code to the counter array (U3 through U7) program inputs. When a count of 9998 is reached in U4 through U7, the next clock pulse into the counter array will load the switch program. Since the state of U8 is at 9, the resultant carry output from U8-15 also allows U8 to load a program from the counter encoder into U8. The program received by U8 is the 9's complement of the switch setting multiplier plus 1. In this case, the synthesizer is operating in range B (table 2-2), N is 2, and the multiplier 2 N is 4. The 9's complement of 4 is 5, so the counter encoder programs U8 with 5 + 1, or 6. The counter array continues to count, and each successive count of 9998 results in reloading the switch setting and advancing the state of U8. At the end of the third switch setting count cycle, U8 is advanced to a state of 9 which, in conjunction with the high output of U9-6 satisfies gate UO1 and presents a low to the counter encoder from U10-8. This low causes the counter encoder to present the program constant 62,499 (9's complement of 37,500) to the counter arra3y and a program 9 to U8. The next count of 9998 in U4 through U7 has several effects. The counter encoder program is loaded, and the carry pulse from U8-15 allows Ut9-6 to toggle back to a low state as well as steering U9-2 high on the next clock pulse. Now, during the 37,500 count, the low output of U9-6 holds U10-8 high even through U8 is in the 9 state, and switch settings are reapplied to the counter array program inputs. The output of U9-3 is used to control the sample function in the phase detector. This output, which was steered high at the beginning of the 37,500 count, is steered low by U1-2 when a count 6480 is decoded at U211. Thus, U9-2 is high for 231 (6480-6249) cycles of the + 10 counter (U11) output, resulting in a 52±10 μsec pulse which repeats each time the divider process goes through a complete cycle.

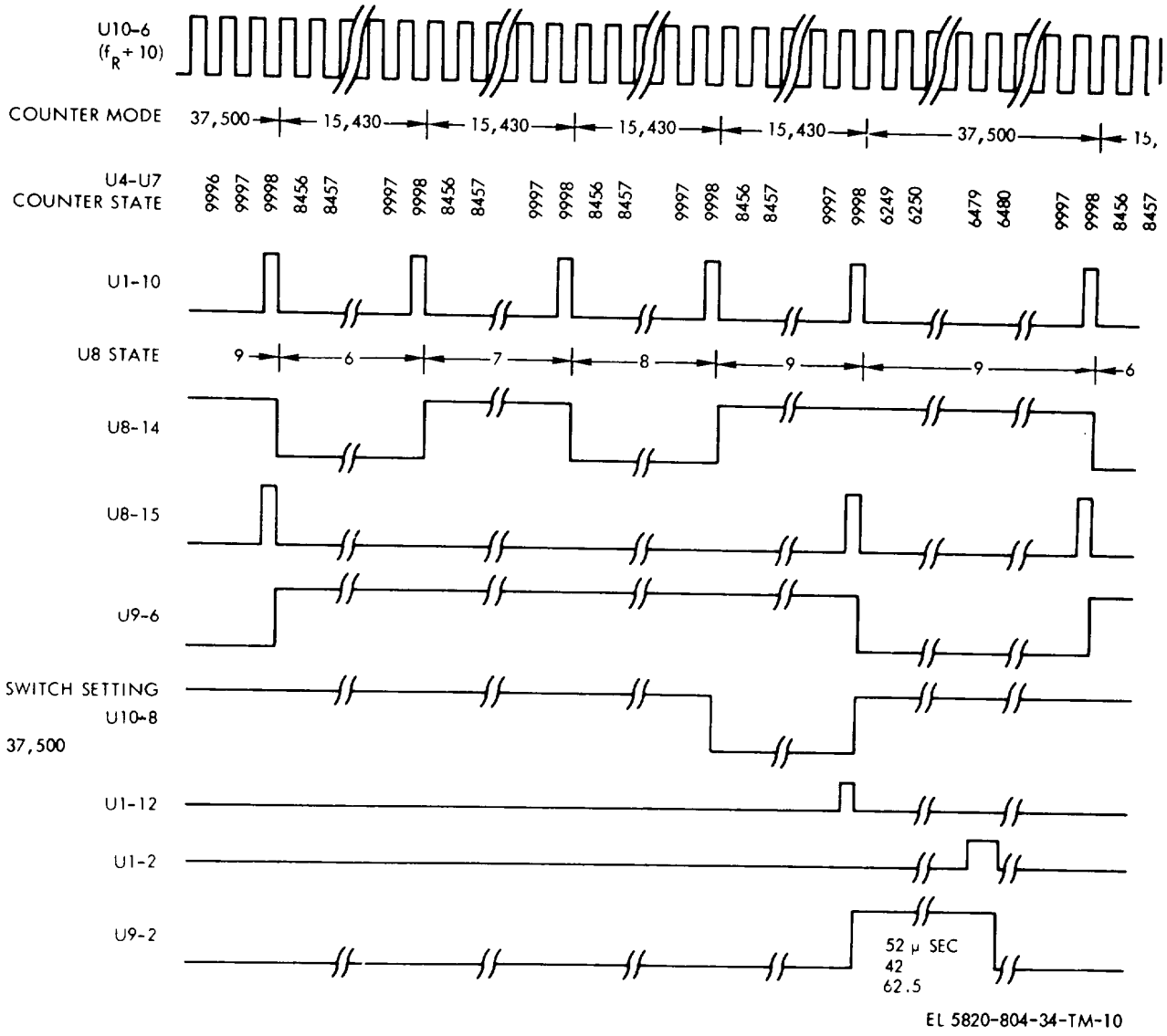

Figure 2-10. Programmable divider, timing diagram

(6) The inverters of U12 route the + 1, + 10, + 100 controls signals from the INPUT DATA RATE switches to the divider circuits on the reference divider card.

h. Counter Encoder (fig. FO-13). The counter encoder, when enabled, gates the 9's complement 20bit code from the five digital INPUT DATA RATE thumbwheel switches (4 bits per switch) to preload the programmable divider card. When thumbwheel switch inputs are inhibited, the counter encoder output is a binary equivalent of the decimal 62499 (9's complement of 37500). The multiplier control section of the counter encoder is programmed by the three most significant thumbwheel switch settings. These digits are examined to determine proper encoding for the programmable divider multiplier section and the binary counter on the reference divider. When inhibited, multiplier coding is (1001).

(1) Circuits U1 through U4, U7, and U12 through U13 provide for gating of the thumbwheel switch 9's complement code to the programmable divider when enabled by the load signal received vi P1-12. Each input is either inverted twice or not a all to produce no change when the counter encoder is enabled by a high on P1-12. The NAND and AND gates, however, provide a binary equivalent of the decimal 62499 to the programmable divider when the switch inputs are inhibited by a low on P1-12.

The outputs are tabulated in table 2-5.

Table 2-5. Counter Encoder Program Outputs

Digit	Bit Pin		(P1-12 low) constant code
	2^0	P1-31	1
1	2^1	P1-26	0
(least significant)	2^2	P1-62	0
	2^3	P1-67	1
	2^0	P1-33	1
2	2^1	P1-28	0
	2^2	P1-64	0
	2^3	P1-32	1
	2^0	P1-39	0
3	2^1	P1-7	0
	2^2	P1-9	1
	2^3	P1-6	0
	2^0	P1-3	0
4	2^1	P1-45	1
	2^2	P1-13	0
	2^3	P1-55	0
	2^0	P1-57	0
5	2^1	P1-11	1
(most significant)	2^2	P1-48	1
	2^3	P1-21	0

(2) To program the multiplier section of the programmable divider and for control of the binary counter on the reference divider, 4-bit digital comparators U1, U5, U6, U8, U9, and U10 are used to examine the three most significant digits of the thumbwheel switch outputs. Output changes occur at the 50,000, 75,000, and 87,500 points of the 9's complemented binary input to the counter encoder (see table 2-6). The digital comparators are arranged to detect these numbers and provide the correct output code. Comparator U8 controls the change at the 50,000 point. The most significant thumbwheel switch digit (4-bits) is applied to the AO through A3 inputs of the comparator and the B inputs are tied to a fixed count of 5 (binary 1010). Since the A > B input (pin 4) to this comparator is high while the other cascade inputs are low, and A = B output is impossible. The comparator A > B output goes high when the most significant digit is equal to or greater than a binary 5 (switch setting > 4). The code change occurring at 75,000 is detected by comparators U5 and U9 connected in cascade. Connections to U5 are identical to those of U8 except the second most significant digit is examined for a 5 or greater. The outputs of U5 are connected to the cascade inputs of U9 while the AO through a A3 inputs are connected to the most significant digit. The BO through B3 inputs of U9 are connected such that the comparator examines inputs for a magnitude equal to or greater than 7. The code change at 87,500 is similarly detected by cascaded comparators U1, U6 and U10 which are connected to detect the digits 5, 7, and 8, respectively. Gates U14 and U15 provide the appropriate output codes to the synthesizer as indicated in table 2-7.

Table 2-6. Counter Encoder Range Decoding

Range	Thumbwheel switch settings	Counter encoder binary inputs	Comparator outputs					
			UB-7	UB-5	U97	U95	U17	U105
A	10000 to 12499	89999 to 87500	0	1	0	1	0	1
B	12500 to 24999	87499 to 75000	0	1	0	1	1	0
C	25000 to 49999	74999 to 50000	0	1	1	0	1	0
D	50000 to 99999	49999 to 00000	1	0	1	0	1	0

Table 2-7. Multiplier and Divider Control Outputs

Range	N	2N	Multiplier program, Z 9's complement of 2"' +1			Binary Counter Control (÷2N+1)					
			2	P1-71	P1-61	P1-29	P1-35	÷2 P1-59	÷4 P1-24	÷8 P1-60	÷16 P1-46
A	3	8	2	0	0	1	0	1	0	0	0
B	2	4	6	0	1	1	0	0	1	0	0
C	1	2	8	1	0	0	0	0	0	1	0
D	0	1	9	1	0	0	1	0	0	0	1
P1-12 low			9	1	0	0	0	1	-	-	-

i. 15 MHz Amplifier (fig. FO-14). The 15 MHz amplifier card contains a current to voltage amplifier, an RF amplifier, a bandpass filter, and an attenuator. The current to voltage amplifier receives the control input from the bit synchronizer and provides a correction voltage to the 15 MHz VCO. The remainder of the circuits on the card receive the output of the VCO and provide amplification and filtering of the 15 MHz input to the mixer.

(1) The current-to-voltage amplifier, AR1, receives the control current output of the bit synchronizer digital/analog converter. AR1 produces an output voltage proportional to the input current with a scale factor of 3.8 V/ma. The resultant correction voltage output from AR1 is routed to the control input of the 15 MHz VCO.

(2) The output of the 15 MHz VCO is received through a 6 dB attenuator formed by resistors R14, R15. and R16 and applied to the two stage RF amplifier. This is the same type amplifier as used in the 45 MHz amplifier except that it has no input operational amplifier stage; therefore, the gain is fixed at approximately 24 dB. The amplifier output, at approximately 19 dBm, is applied across a 6 dB attenuator formed by resistors R1, RS, and R6 to bandpass filter FLI. The filter center frequency is 15 MHz, the 20 dB bandwidth is 9 MHz, and the 40 dB bandwidth is 15 MHz. The filter output is applied through 3 dB attenuator R2, R7, and R8 to the mixer/output amplifier.

j. Mixer/Output Amplifier (fig. FO-15). The mixer/output amplifier card contains a double balanced mixer that accepts a 45 +10 MHz input and a 15 MHz input to develop a 30 ±10 MHz output. The card also contains a three stage RF amplifier and attenuators for matching and level setting. The output (20 to 40 MHz) is routed to a a low pass filter on the reference oscillator card.

(1) The high level 45 +10 MHz input is applied across a 2 dB attenuator formed by R8, R11 and R12 and provides a +7 dBm input to mixer U1. The 15 MHz input is applied across a 6 dB attenuator formed by R23 through R25 to provide a 0 dBm input to the mixer. The difference frequency output, 20 to 40 MHz, is applied across a 26 dB attenuator formed by resistor R9, R10, and R13 through R15 to the RF amplifier.

(2) This three stage amplifier is identical to the circuit used on the 45 MHz amplifier card. The amplifier output is applied through a low pass filter on the reference oscillator card to the programmable decade and binary counters on the reference divider card.

k. 15 MHz VCO. The 15 MHz VCO, A2Y2, is a Vectron Laboratories, Inc., VCO part number 2721208. The center frequency stability is 1 kHz/day. The control voltage input is +5.0 volts peak, producing a deviation of +9200 kHz. A screwdriver adjustment permits maintenance adjustment of center frequency.

2-6. Coders and Interface

a. General.

(1) The coder switch section of the coders and interface (fig. FO-1) permits selection of bit syn data or bypass data, provides differential encoding when selected, and provides gating for selection of externally error coded data or data with no error coding.

(2) Bypass data from the input circuits and data from the bit synchronizer are applied to the input data gates. When the STD/CLK/ICF switch is in the CLK position, bypass data is gated to the differential encoder; in either of the other switch positions, bit synchronizer data is gated to the encoder. If the differential coder is enabled (DIFF ENCODE switch in ON position), each data ONE bit received at the input develops a transition at the output while each data ZERO bit produces no transition. When the DIFF ENCODE switch is set to OFF, the data passes through the coder unchanged except for a one-bit period delay. The output of the differential coder is applied to the no error coding gates and, via the coder interface card, to the external error coder. When the TRANSMIT ERROR CODING switch is set to NONE, data an clock are gated directly from the differential coder through the data and clock OR gates to the data out flip-flop.

(3) Data, bit rate clock, and two times bit rate clock are routed via the coder interface to an external coder. If the TRANSMIT ERROR CODING switch is set to EXT, externally coded data (symbols) and accompanying clock are returned via the coder interface and applied through the data out flip-flop. Any of the external coder interface clock signals may be inverted by switches located on the coder interface card. In all coding modes, the data output of the data out flip-flop and clock from the clock OR gate are routed to the LOS/ cable driver

b. Coder Switch (fig. FO-16). The coder switch consists of encoder switching logic and decoder switching logic. Only the encoder switching logic functions are discussed in this paragraph; the decoder switching logic functions are discussed in paragraph 2-11. The coder switch receives transmit data from the bit synchronizer or directly from l input interface and, if selected, provides differential encoding. The differential coder output is provided for use by an external error correcting coder. The coder switch also provides the selection of the resulting externally encoded data, or the direct

output of the differential coder for subsequent processing by the LOS/cable driver.

(1) When the STD/CLK/ICF switch is in the CLK position (P1-16 grounded), output pin 4 of inverter U14 is high to enable pin 4 of AND gate U1. In this mode, bypass data from the input interface card is gated to the differential coder formed by adder U4 and one flip-flop section of U5 and the transmit bit sync data input (P1-42) is disabled. In any other switch position, data from the transmit bit synchronizer is gated to the differential coder.

(2) In this application, bit rate clock is applied to both P1-9 and P1-43, and twice bit rate clock is applied to both P1-52 and P1-53. Because either U1-1 or U1-10 is high, depending on the input to U14-3, bit rate clock is always present at U1-8 and twice bit rate clock is always present at U8-6.

(3) When differential encoding is selected (DIFF ENCODE switch is set to ON), ground is applied to the pin I input of adder U4. This adder is also grounded at a second input (pin 3) and data is applied to the third (pin 4); Therefore, the sum output will be the same as the data input. Thus, JK flip-flop U5 will toggle each time a negative clock trasition occurs when data is a logic ONE and will not switch when data is a logic ZERO. If differential encoding is not selected, a logic ONE is applied to one input of the adder. In this mode, the data is added to ONE (effectively inverted) and applied to the K input of the flip-flop. Thus, the data simply shifts through flip-flop U5. The Q putput of U5 is routed via P1-51 to the external error correcting coders and is also applied to pin 13 of AND gate U2.

(4) Selection of the signal to be processed is accomplished by AND gates U2 and U6, and the OR gates of U7. These gates are controlled by the TRANSMIT ERROR CODING switch.

(a) When the ERROR CODING switch is in the EXTERNAL position, all AND gates of U2 and U6 are inhibited since P1-15 and P1-24 are both high, forcing U3-6 and U2-8 low. Placing the TRANSMIT ERROR CODING switch in this position applies a ground to P1-10, causing a high output from U14-6 which is used to enable the external encoder line receivers on the coder interface card. Data (P1-7) and clock (P1-46) from the external coder via the coder interface card are applied to the data out flip-flop U5 through the OR gates of U7.

(b) If the ERROR CODING switch is in the NON position, P1-10 and P1-24 are both high, and Pl-15 is grounded. The resultant low output from U14-6 disables the external encoder line receivers on the coder interface card and forces the signals at P1- 7 and P1-46 high. The resultant low at U6-2, U6-3 and U2-1 disables these gates. The resultant high at U2-12 and U2-4 allows the differential encoder output (U5-9) and bit rate clock (Ui4-21 to be gated to data out flip-flop U5 via the OR gates of U7.

(5) The Q output of flip-flop U5-25 provides data and the output of U7-8 provides the appropriate clock (bit rate or bit rate times two) to the LOS/cabledriver.

c. Coder Interface (fig. FO-17). The coder interface card contains five dual line drivers and two dual line receivers that provide interface between the ICF' modem and the external error coder and decoder.

(1) Circuits U1 through U5 are identical dual line drivers that convert logic inputs to differential outputs. A logic ONE is the off state of the driver and a logic ZERO is the on state (fig. 2-11). A logic ONE is 0 volt while a logic ZERO is between -70 and -135 millivolts, and the drivers have a current sink of between 3.5 and 7 milliamperes.

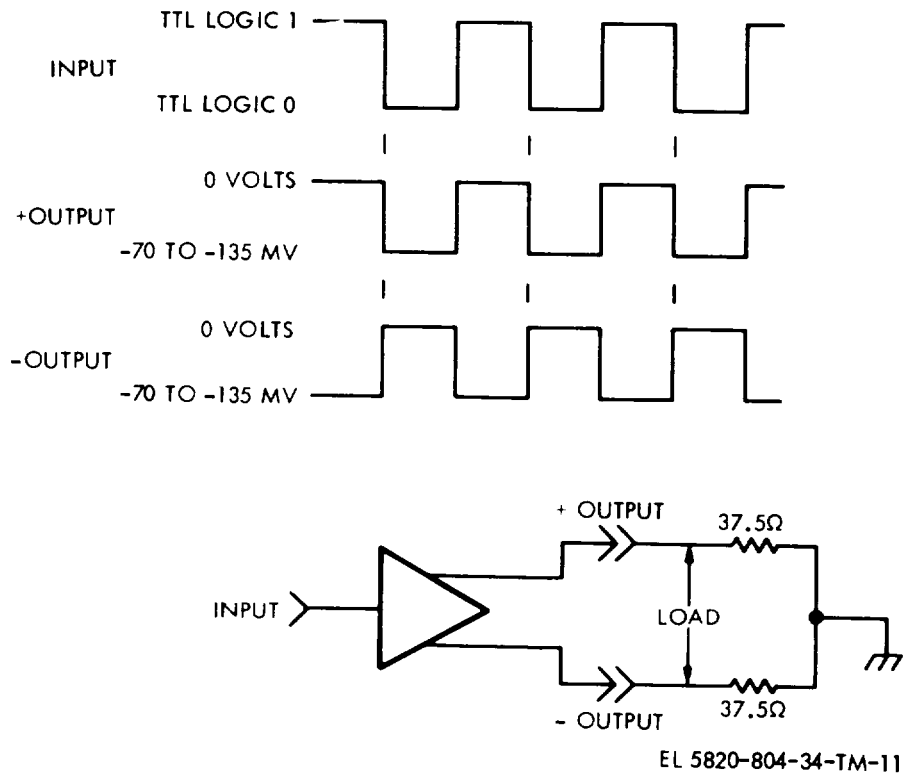

Figure 2-11. Coder interface output.

(2) Line receivers U6 and U7 receive differential input signals such as those generated by line drivers U1 through U5, and produce TTL logic compatible outputs. The outputs switch when a differential input voltage of 25 millivolts is received. Line receiver U6 is enabled by a high on pin 6 only when the TRANSMIT ERROR CODING switch is in the EXT position. Otherwise, the outputs remain high when a low is applied to pin 6. Line receiver U7 functions the same way as U6 except that it is enabled only when the RECEIVE ERROR CODING switch is in the EXT position.

(3) Switches S1 through S6 provide the capability of inverting the appropriate balanced input/ output signals. On all switches, position 1 provides the normal polarity and position 2 provides the inverted polarity.

2-7. Drivers

a. General. The ICF modem contains two types of drivers (fig. 2-12). The drivers on the LOS/cable driver card convert the output of the coders and interface to a bipolar NRZ format for transmission over an appropriate interconnect facility (LOS or cable). The drivers on the line driver card retain the NRZ format received from the coders and interface, for its interface with the interconnect facility. Collectively, the circuits of the drivers are contained on three cards as shown in figure 2-12. The 75-ohm unbalanced, the 50-ohm unbalanced, and the LOS out- puts are developed on the LOS/cable driver card, and are routed directly to the appropriate connector pins on the rear panel of the modem. The two 75- ohm balanced outputs, one from the line driver card (A2A1A1A21) and the other from the LOS/cable driver card (A2A1A2A3), share the same set of out- put pins on the modem rear panel connector. The required switching for selecting either of the two 75-ohm balanced signals is located on the NRZ inter- face card (A2A1A2A2), from which the selected signal is applied directly to the output connector pins on the modem rear panel.

b. LOS/Cable Driver (fig. FO-18). The LOS/ cable driver (A2A1A2A3) receives NRZ-L data and clock from the coder section of the coder switch and develops bipolar NRZ outputs at + 23, + 10 or 0 dBm to drive cable loads of 50 ohms and 75 ohms unbalanced and 75 ohms balanced. A 75 ohm unbalanced output is also provided at power levels of -2, -12, or -22 dBm to drive an LOS microwave link. A test output is also routed to the LOS/cable receiver decoder (A2A1A2A1).

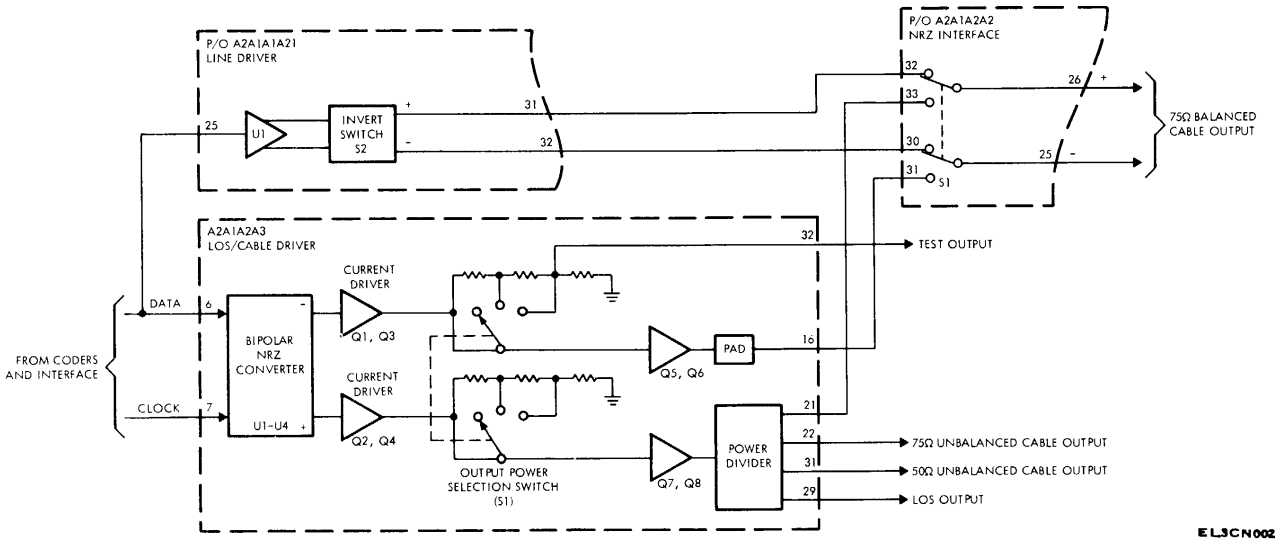

Figure 2-12. Drivers, functional block diagram.

(1) The input logic, U1 through U4, converts the NRZ-L data such that the output amplifiers develop bipolar NRZ data. The bipolar NRZ format is one in which ONE bits are represented by alternate positive and negative levels while ZERO bits are represented by ground levels. When the data input is high (logic ONE), the outputs from inverters of U1 steer flip-flops of U2 such that the input ONE is shifted into U2 (Q output pin 5) and U2 (Q output pin 9) is allowed to toggle to the opposite state. Outputs of U3 then steer flip-flops of U4 to provide the appropriate positive or negative control inputs to the amplifiers. When the data input is low (logic ZERO), flip-flop U2 (Q output pin 5) is steered to a zero and both AND gates of U3 are inhibited. The resultant high outputs from AND gates of U3 steer the Q out- put pin 7 of flip-flop U4 low and the Q output pin 6 of flip-flop U14 high. Thus, an input logic ONE causes the states of U4-7 and U4-6 to be identical highs or lows depending on the state of U2, while an input ZERO forces U4-7 low and U4-6 high.

(2) Transistors Q1 and Q2, Q3 and Q4 form a complementary pair of differential current mode switches with OR'ed collectors which assume the states indicated in table 2-8. The output from the junction of Q2 and Q4 is either a positive or negative current, or ground when both transistors are on and the source current equals the sink current. The out- put from the junction of Q1 and Q3 is either a positive or negative current with the opposite polarity from the other current output (Q2 and Q4), or ground when both transistors are off. The voltage levels at the outputs of the current mode switches (which are equal and opposite), and thus the power outputs of the circuit are controlled by using switch S1 to change the load resistances. The link test out- put is taken directly from the attenuator outputs while the ICF data is applied to amplifier/line drivers Q5, Q6 and Q7, Q8. The outputs of the line drivers then drive the ICF cable or LOS microwave link through the appropriate impedance matching resistors.

c. Line Driver (fig. FO-20). The line driver card contains two identical sections to convert logic level inputs to balanced outputs to interface with external equipment.

(1) The logic level inputs to the line drivers are applied through hex inverters of U1 to switching transistors that drive the differential amplifiers. Since the two driver circuits are identical, only the circuit associated with the P1-16 input is discussed. Transistor Q2 is biased such that when U1-4 is low, Q2 is on, and the current through R4 provides base drive to Q1, which is a saturating switch. Since Q3 receives its base drive from Q1 collector, Q3 will be off. The current through R7, in this case will flow through R2 through CR6, causing Q5 to supply no base drive current to Q7. Since Q7 is off, Q6 will be on because of the base current received through R6The resultant output with S1 in position 1, is P1-22 high and P1-21 low, R8, and R14. When U1-4 goes high, transistor Q4 and diode CR5 will back-bias diode CR6 and cause CR3 to conduct, reversing the states of all the remaining transistors and therefore the outputs.

(2) The amplifier outputs are routed through switches that permit polarity inversion to the output connectors. Each amplifier output is also connected to one section of line receiver U2. The line receivers reconvert the signals to logic-level outputs for test purposes.

d. *NRZ Interface* (fig. FO-18.1). The two 75-ohm balanced driver outputs are applied to the NRZ interface card. The bipolar NRZ outputs are routed to input pins 31 and 33, and the NRZ outputs are routed to input pins 30 and 32. The position of switch S1 determines which output is selected as the modem output. When S1 is in position 1, the 75-ohm balanced outputs from the LOS/cable driver card are applied to the modem output connector. When S1 is in position 2, the outputs from the line driver are routed to the modem output connector.

2-8. Receivers

a. General. The receiver circuits (fig. 2-13) accept an input from the interconnect facility. The LOS/cable input circuits provide cable equalization and also convert the bipolar NRZ format to logic- level NRZ-L outputs (fig. 2-14). The bipolar NRZ format represents ONE bits by alternating positive and negative voltages. Positive and negative comparators in the LOS/cable receiver decoder detect the voltage excursions and develop ICF1 and ICF2 signals which are OR'ed by the input interfaces card to develop logic level ONE bits. The bipolar NRZ ZERO bits are represented by ground levels. In this case, the outputs of both comparators are high with a resultant logic level ZERO from the OR gate (ICF

Table 2-8. Balanced Amplifier Drive

U4-7	U4-6	Q1	Q2	Q3	Q4
1	1	OFF	ON	ON	OFF
0	0	ON	OFF	OFF	ON
0	1	ON	OFF	ON	OFF

data). In the test mode, a similar bipolar NRZ link test signal from the LOS/cable driver is relay switched to the comparators and is inserted in place of the ICF signals. The LOS, 50-ohm unbalanced, and 75-ohm unbalanced inputs to the modem are routed directly to the LOS/cable receiver and de- coder card (fig. 2-13). The 75-ohm balanced input is applied to the NRZ interface card, where the input signal is switched to either the 75-ohm balanced receiver on the LOS/cable receiver and decoder card or is sent to the NRZ receiver on the NRZ interface card. After the LOS, balanced, or unbalanced input signal has been processed by the receiver circuits, the receiver output is sent to the receive bit sync. Relay K1 provides for the application of a test signal to the NRZ receiver.

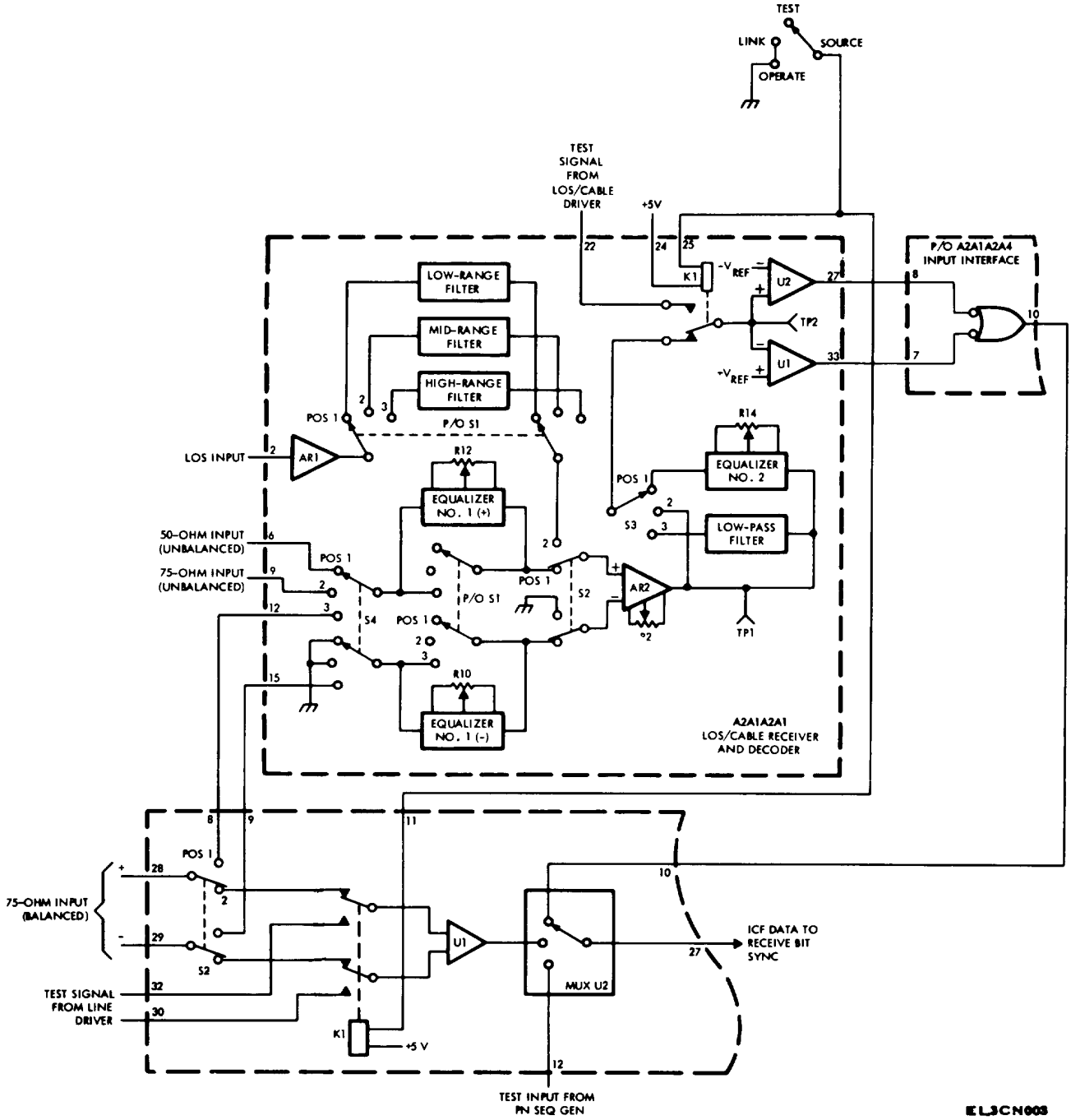

Figure 2-13. Receivers, functional block diagram.

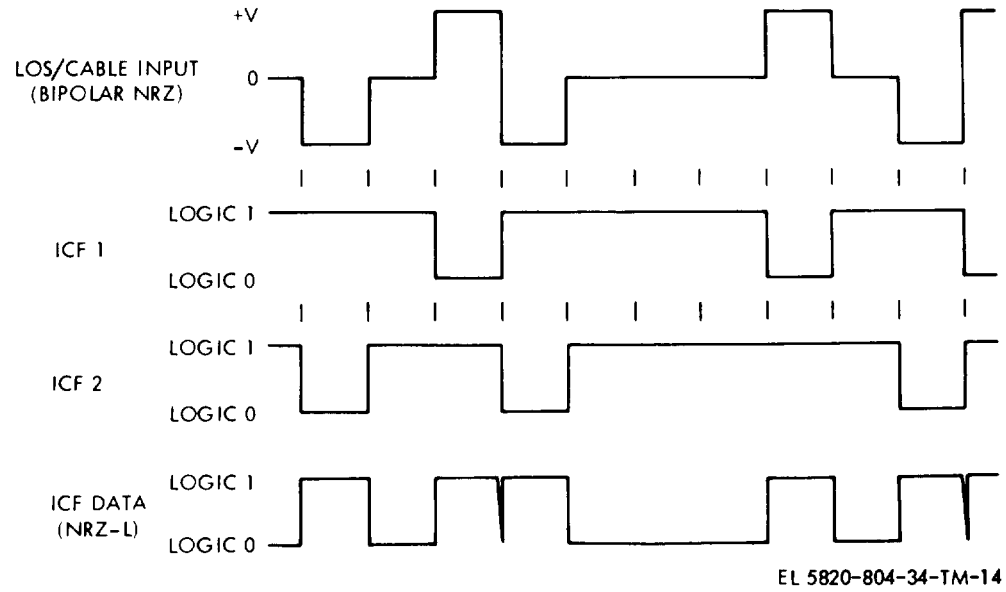

Figure 2-14. Bipolar NRZ to NRZ conversion.

b. LOS/Cable Receiver and Decoder (fig. FO-19). The LOS/cable receiver and decoder provides input selection, filtering, equalization, amplification, and decoding of the received signal.

(1) The input selection, filtering, and equalization functions of the circuits are controlled by four card-mounted switches, S1 through S4. The functions of these switches are given in table 2-9.

Table 2-9. Operation of LOS/Cable Receiver and Decoder Selection Switches

Switch	Position	Function
A2A1A2A1S1	1	Selects input filter for use at input data rates from 19.200 kb/s to 225.00 kb/s if LOS microwave input is used; selects no first stage of equalization if any cable input is used.
	2	Selects input filter for use at input data rates from 225.01 kb/s to 1.8000 Mb/s if LOS microwave input is used.
	3	Selects input filter for use at input data rates from 1.8001 Mb/s to 5.0000 Mb/s if LOS microwave input is used; selects use of first stage of equalization if any cable input is used.
A2A1A2A1S2	1	Selects operation with cable inputs.
	2	Selects operation with LOS microwave input.
A2A1A2A1S3	1	Selects use of second stage of equalization at decoder input.
	2	Selects use of no equalization or filtering at decoder input.
	3	Selects use of low pass filter at decoder input.
A2A1A2AIS4	1	Selects 50-ohm unbalanced cable input.
	2	Selects 75-ohm unbalanced cable input.
	3	Selects 75-ohm balanced cable input.

(2) If an LOS input (P1-2) is used, AR1 provides a stage of preamplification, with a gain of 25 dB. The output of AR1 is applied through one of the switchable lowpass filters to S2. The lowpass filters consist of resistor R5 and the capacitor combinations shown below:

S1 Position	3 dB Bandwidth	Capacitors	Capacitance
1	55 kHz	C9 + C2	510 pf
2	3.6 MHz	C9 + C5	95 pf
3	10MHz	C9	39 pf

(3) If one of the cable inputs is used, S4 is used for input selection. The selected input is routed

through S1, which provides the capability of switching into the circuit a stage of cable equalization (L2, L4, R10, R12) and then to S2 which selects either the LOS or the cable input for further processing.

(4) The input selected by S2 is amplified by AR2. Resistor R2 permits adjustment of the gain of AR2 to obtain the proper output level (2.4 V p-p at TP1) regardless of the input signal level. Switch S3 permits the selection of a second stage of cable equalization (L3, R14), a lowpass filter (R15, C12) which eliminates system noise above 15 MHz, or a straight through path to the next stage.

(5) Data from AR2 is applied through contacts of relay K1 (energized except when SOURCE switch is in TEST position) to differential comparators U1 and U2. The threshold of comparator U1 is set to + 03 volt and the threshold of comparator U2 is set to -0.3 volt. When a ONE bit is received, the threshold level of one of the comparators is exceeded, with a resultant ground level output from that comparator. When ZERO bit is received, both comparators produce positive outputs. (These signals are OR'ed in the input interface card to produce NRZ coded data.)

(6) When the SOURCE switch is set to the TEST position, relay K1 is deenergized by an open at P1-25 and the test output from the LOS/cable driver is routed to the comparators.

c. NRZ Interface (fig. FO-18.1). The NRZ interface provides switching for the 75-ohm balanced, bipolar NRZ and NRZ input signals, and also provides the receiver circuits for NRZ format input signals.

(1) Card-mounted switch S2 is used to switch the balanced input signal, which is received on P1-28 and P1-29. If the balanced input signal is in a bipolar NRZ format, S2 is placed in position 1 so that the signal is routed to the LOS/cable receiver and decoder through P1-8 and P1-9. For a balanced input signal that is in a NRZ format, S2 is set to position 2, and the input signal is applied to the NRZ receiver U1 through test relay K1. The output of the NRZ receiver is routed through the digital multiplexer U2 to the receive bit synchronizer via output pin P1-27.

(2) Relay K1 serves as a means of connecting the NRZ driver output on P1-30 and P1-32 to the input of NRZ receiver U1 for modem self-testing. Relay K1 provides a path for looping the NRZ driver outputs into the NRZ receivers, whenever the SOURCE switch on the front panel is set to the TEST position, which deenergizes the relay.

(3) The digital multiplexer U2 selects one of three inputs to the receive bit synchronizer, de- pending on the position of card-mounted switch S2 and the TEST switch located on the modem front panel. When S2 is in position 1, the output of the LOS/cable receiver on P1-10 is selected and applied to the input to the receive bit synchronizer through P1-27. When S2 is in position 2, the output of the NRZ receiver U1 is applied to the input of the receive bit synchronizer through P1-27. During self- test, when the TEST switch is in position 3, a test sequence presented on P1-12 is selected and applied by the multiplexer to the input of the receive bit synchronizer through P1-27.

2-9. Receive Bit Synchronizer

The operation of the receive bit synchronizer is identical with the transmit bit synchronizer (para 2-4). A functional block diagram of the receive bit synchronizer is shown in figure 2-15.

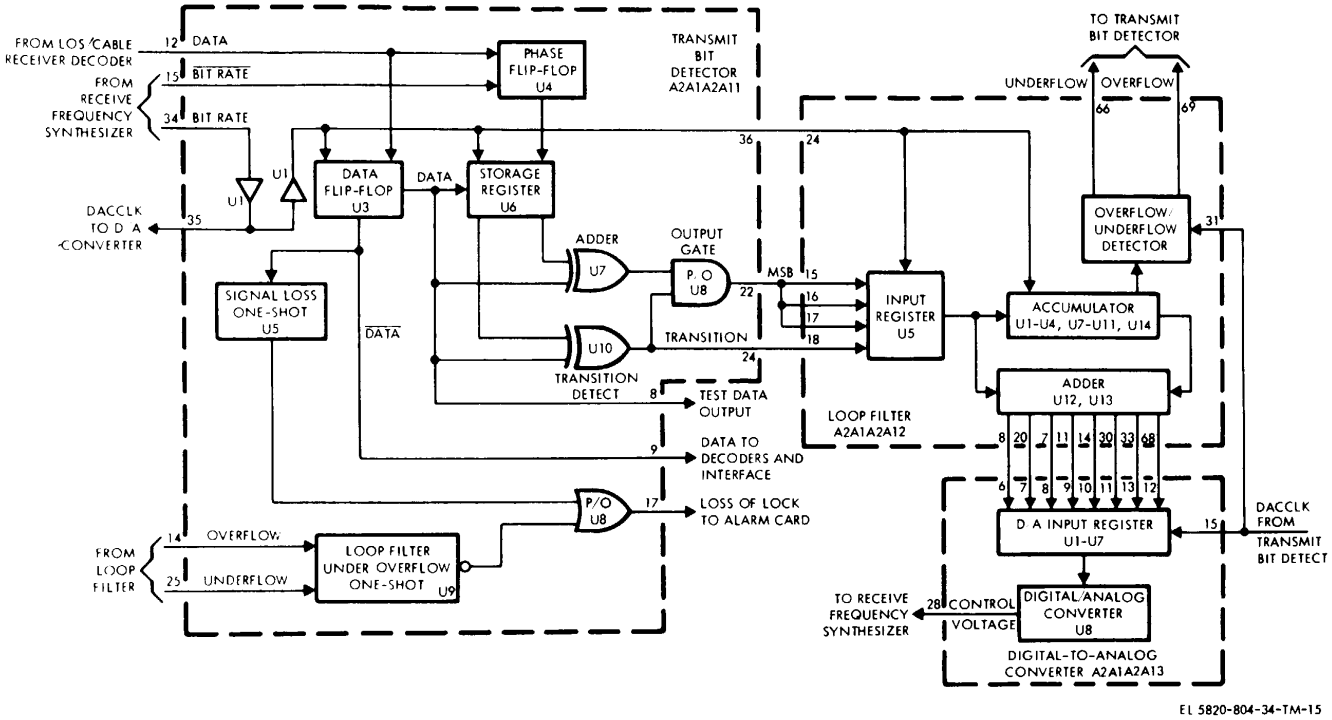

Figure 2-15. Receive bit synchronizer, functional block diagram.

2-10. Receive Frequency Synthesizer

The operation of the receive frequency synthesizer, which is controlled by the RECEIVE SYMBOL RATE switches, is identical to the transmit frequency synthesizer (para 2-5). A functional block diagram of the receive frequency synthesizer is shown in figure 2-16.

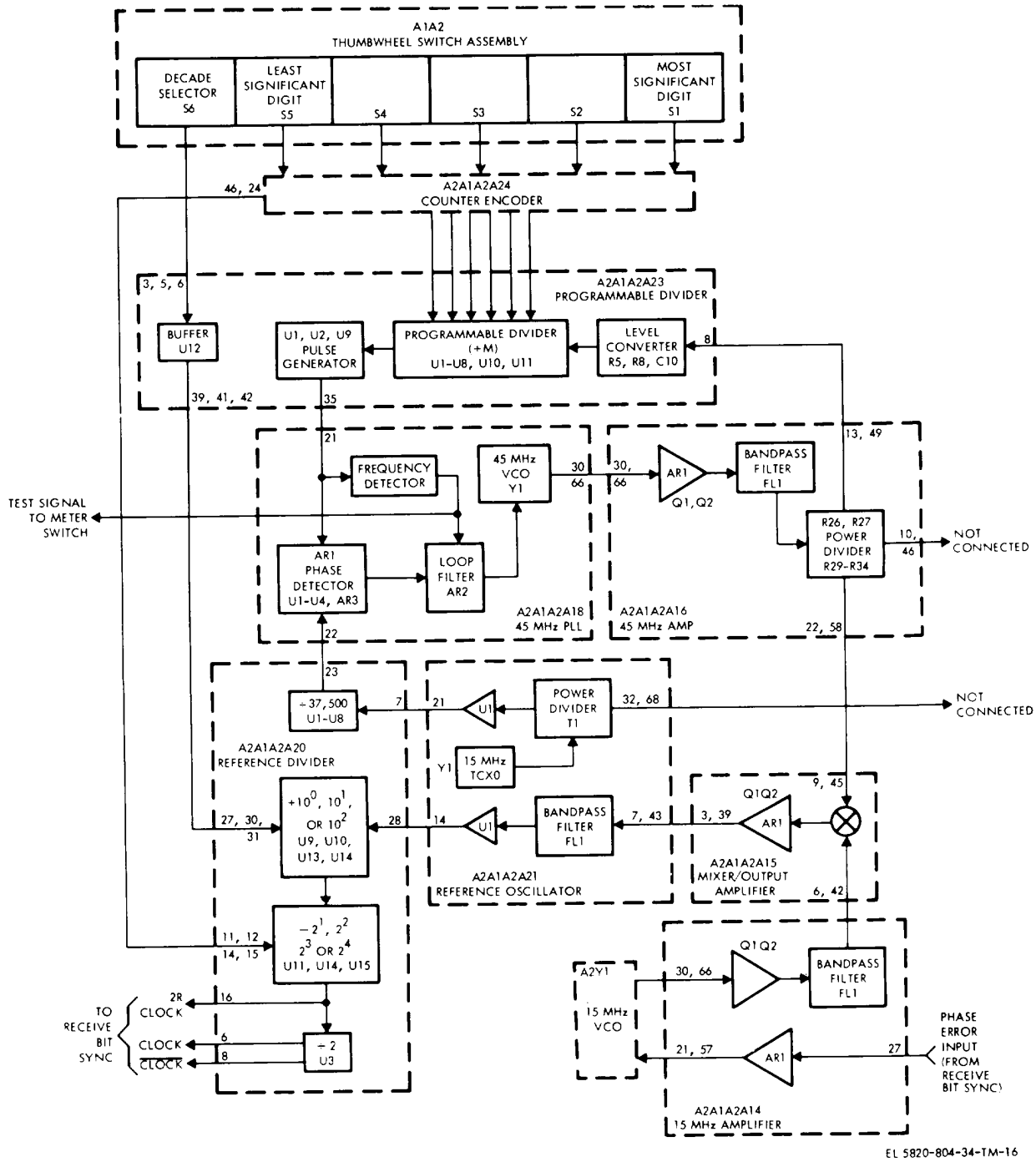

Figure 2-16. Receive frequency synthesizer, functional block diagram.

2-11. Decoders and Interface

a. General. The decoders and interface (fig. 2-17) operates in one of two primary modes dependent upon the setting of the RECEIVE ERROR CODING switch. When the RECEIVE ERROR CODING switch is set to EXTERNAL, the decoders and interface supplies symbol rate clock and symbols from the receive bit synchronizer to the external decoder. The external coder/decoder then returns decoded data and data rate clock to the decoders and interface. When the RECEIVE ERROR CODING switch is set to NONE, the external decoder is bypassed. As a secondary mode, the output of the decoder switching function is either differentially decoded or not, depending on the setting of the DIFF DECODE switch.

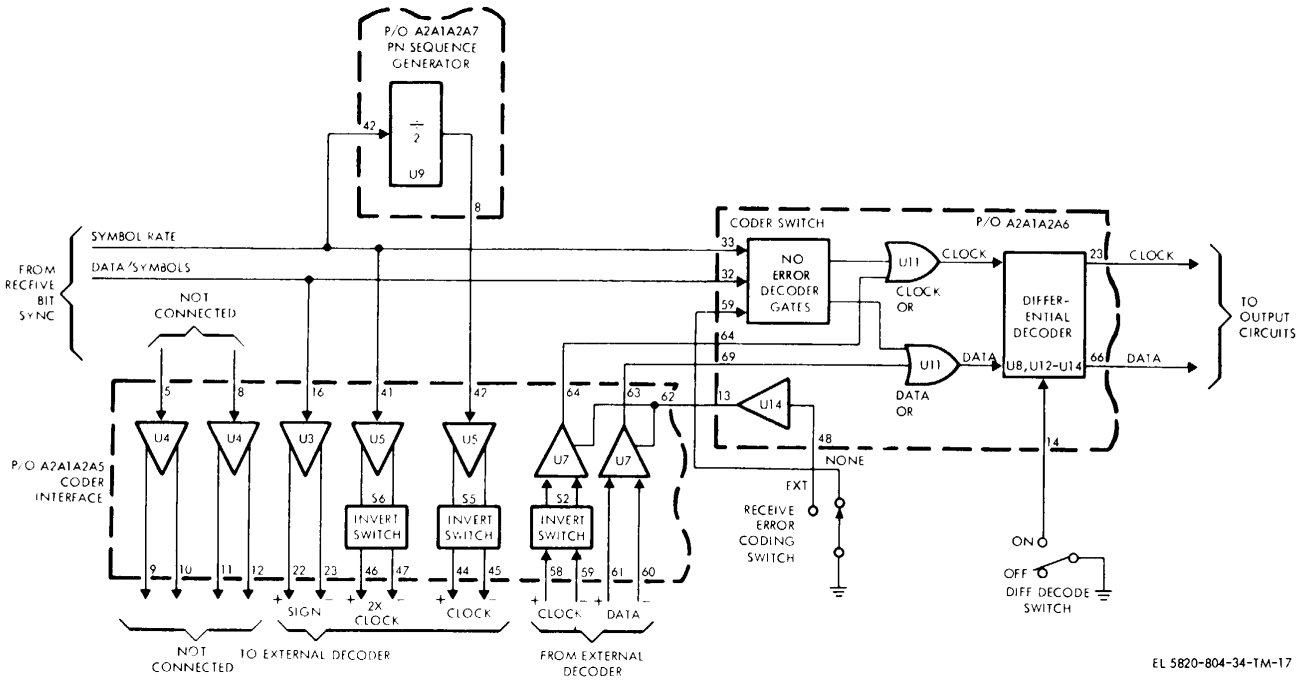

Figure 2-17. Decoders and interface, functional block diagram

(1) The inputs and a one-half symbol rate clock generated by a flip-flop located on the PN sequence generator card are provided to the external decoder via 3 line drivers on the coder interface card. When the RECEIVE ERROR CODING switch is in the EXTERNAL position, an inverter input on the coder switch card is grounded, which enables two line receivers on the coder interface card and allows decoded data from the external decoder to be routed to the differential decoder.

(2) When the RECEIVE ERROR CODING switch is in the NONE position, the external decoder is bypassed and the differential decoder operates directly on the data and clock from the receive bit synchronizer.

(3) The differential decoder receives either externally decoded data or the output from the receive bit synchronizer along with the respective clock signals. With the DIFF DECODE switch in the ON position, the decoder converts input transitions to output ONE's and no transitions to output ZERO's. The differential decoder is bypassed when the DIFF DECODE switch is in the off position. The differential decoder output data, accompanied by clock, is routed to the output circuits.

b. Coder Switch (fig. FO-16). The coder switch consists of encoder and decoder switching logic. Only those functions associated with the decoders and interface are discussed in this paragraph. The encoder switching functions are covered in paragraph 2-6 b.

(1) The decode logic of the coder switch receives data and clock from the external decoder or from the receive bit synchronizer and provides appropriate gating for the selected signals. The decode logic also provides differential data decoding, when selected. When the RECEIVE ERROR CODING switch is in the EXTERNAL position, the external decoder is enabled and data is received via PI-69, OR'ed by U11, and applied to the data input of one flip-flop of U12. The data is loaded by clock from the external decoder received via P1-64 and a second OR gate of U11. When the coder switch is in the NONE position, AND gates of U10 are enabled by the high output of U3-12. In this mode, data and clock from the receive bit synchronizer are received via P1-32 and P1-33, respectively. The bit synchronizer data is then loaded into flip-flop U12 the same way as for the decoded data. The AND gates of U9 are not used since they are alwyas inhibited by the low output of U14-12.

(2) The outputs of data flip-flop U12, flip-flops of U13, adder U4 and gates of U8 provide for differnetial decoding or no decoding as selected by the DIFF DECODE switch. When the switch is in the OFF position, AND gate U8 (pm 9) is enabled by a high output from U14-10. The Q output from data flip-flop U12 is then gated and inverted through U8 to the data input of flip-flop U13 (pin 12). When the decode swithc is set to ON, U8-9 is inhibited and U8-13 is enabled. Decoding is then accomplished by summing the Q output of U12 with the Q output of U13. If no transition has occurred between bits, the flip-flop states will be identical and the sum of the outputs will be a ONE. This ONE bit is inverted through gates of U8 and the data output flip-flop, U13, is loaded with a ZERO. When a bit transition has occurred, the and Q outputs are the same (the flip-flop states are different), their sum is ZERO and output flip-flop U13 is loaded with a ONE. The data and clock outputs from P1-66 and P1-58 are routed to the output circuits.

c. Coder Interface. The coder interface contains the line drivers and receivers necessary to operate with an external error correcting decoder. The operation of the coder interface is discussed in paragraph 2-6 c.

2-12. Output Circuits

a. General. The output circuits generate the necessary output signal characteristics to provide the demodulated data and reconstructed clock to the digital user. A block diagram of the output circuits is shown in figure 2-18. The data and reconstructed clock are provided directly to the digital user via two identical line driver circuits on line driver card A2A1A1A23. The standard data and clock outputs of this card provide 6-volt peak-to-peak balanced signals into a balanced 75-ohm load. The card also contains a dual line receiver to monitor the data and clock outputs and provide signals compatible with the internal test circuits. Line driver A2A1A1A22 provides an identical set of outputs for use by a second digital user, if required.

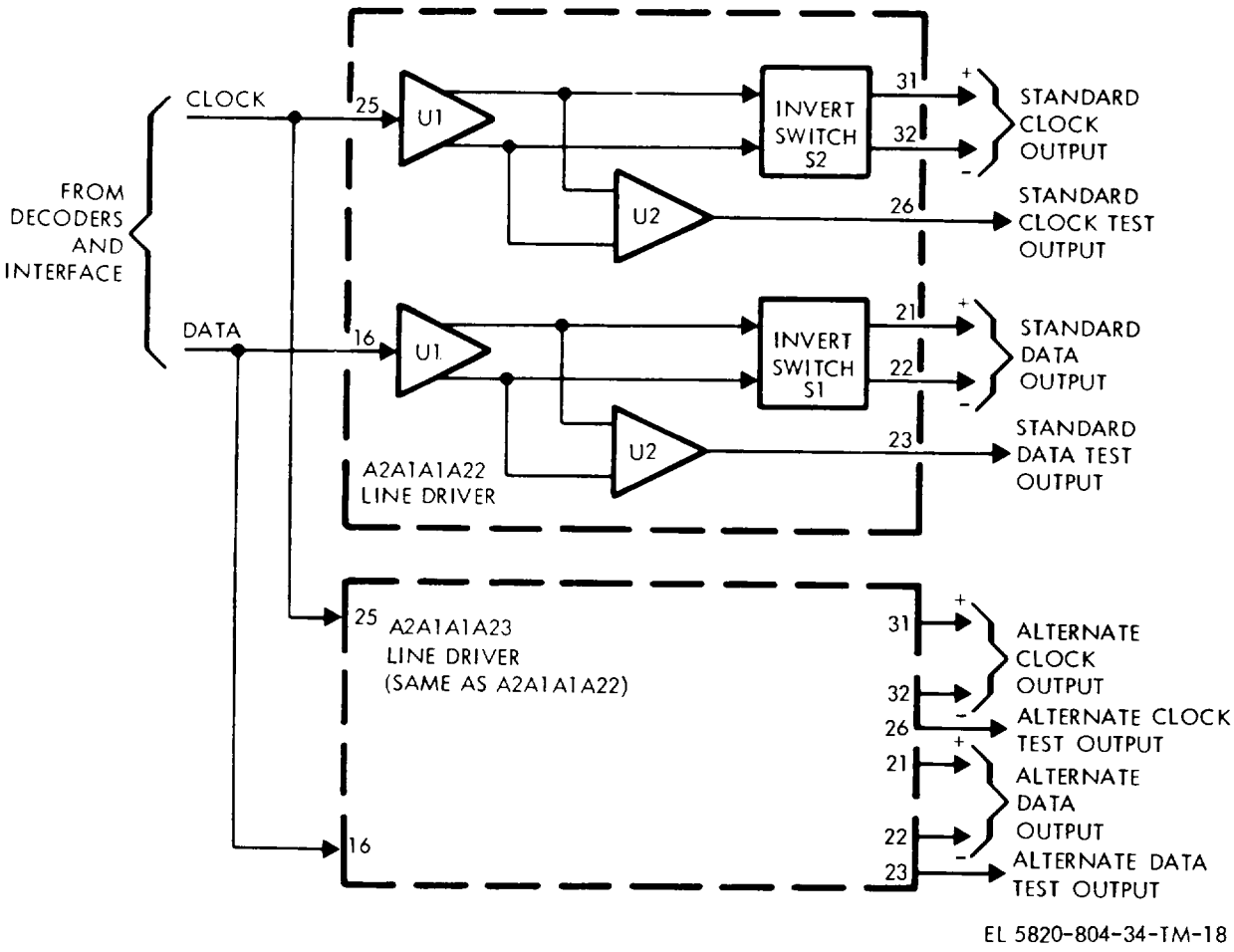

Figure 2-18. Output circuits, functional block diagram.

b. Line Drivers (fig. FO-20). The two line driver cards each contain two identical sections to convert logic level inputs to balanced outputs to interface with external equipment.

(1) The logic level inputs to the line drivers are applied through hex inverters of U1 to switching transistors that drive the differential amplifiers. Since the two driver circuits are identical, only the circuit associated with the P1-16 input is discussed. Transistor Q2 is biased such that when U1-4 is low, Q2 is on, and the current through R4 provides base drive to Q1, which is a saturating switch. Since Q3 receives its base drive from Q1 collector, Q3 will be off. The current through R7, in this case will flow through R2 via CR6, causing Q5 to supply no base drive current to Q7. Since Q7 is off, Q6 will be on because of the base current received through R6, R8, and R14. The resulting output, with S1 in position 1, is P1-22 high, and P1-21 low. When U1-4 goes high, transistor Q4 and diode CR5 will back-bias diode CR6 and cause CR3 to conduct, reversing the states of all the remainving transistors and therefore the outputs.

(2) The amplifier outputs are routed through switches that permit polarity inversion to the output connectors. Each amplifier output is also connected to one section of line receiver U2. The line receivers reconvert the signals to logic level outputs for test purposes.

2-13. Internal Clock Generator

a. General. The internal clock generator is shown in figure 2-19. The operation of the internal clock generator is similar to the equivalent sections of the transmit frequency synthesizer, discussed in paragraph 2-5. The stable clock card receives the programmable reference frequency, f R , and a stable 15-MHz reference signal from the transmit frequency synthesizer, and provides a logic-compatible output of the difference frequency.

This function is equivalent to the function of the mixer/output amplifier card along with the filter and level converter located on the reference oscillator card of the transmit synthesizer. The same reference divider is used, and the reference divider control inputs are connected in parallel with the control lines for the reference divider in the transmit frequency divider. The result, since a stable 15-MHz reference signal is used instead of the 15-MHz VCO output, is a clock signal at the selected INPUT DATA RATE. A line driver provides the clock signal to the digital user as a balanced output.

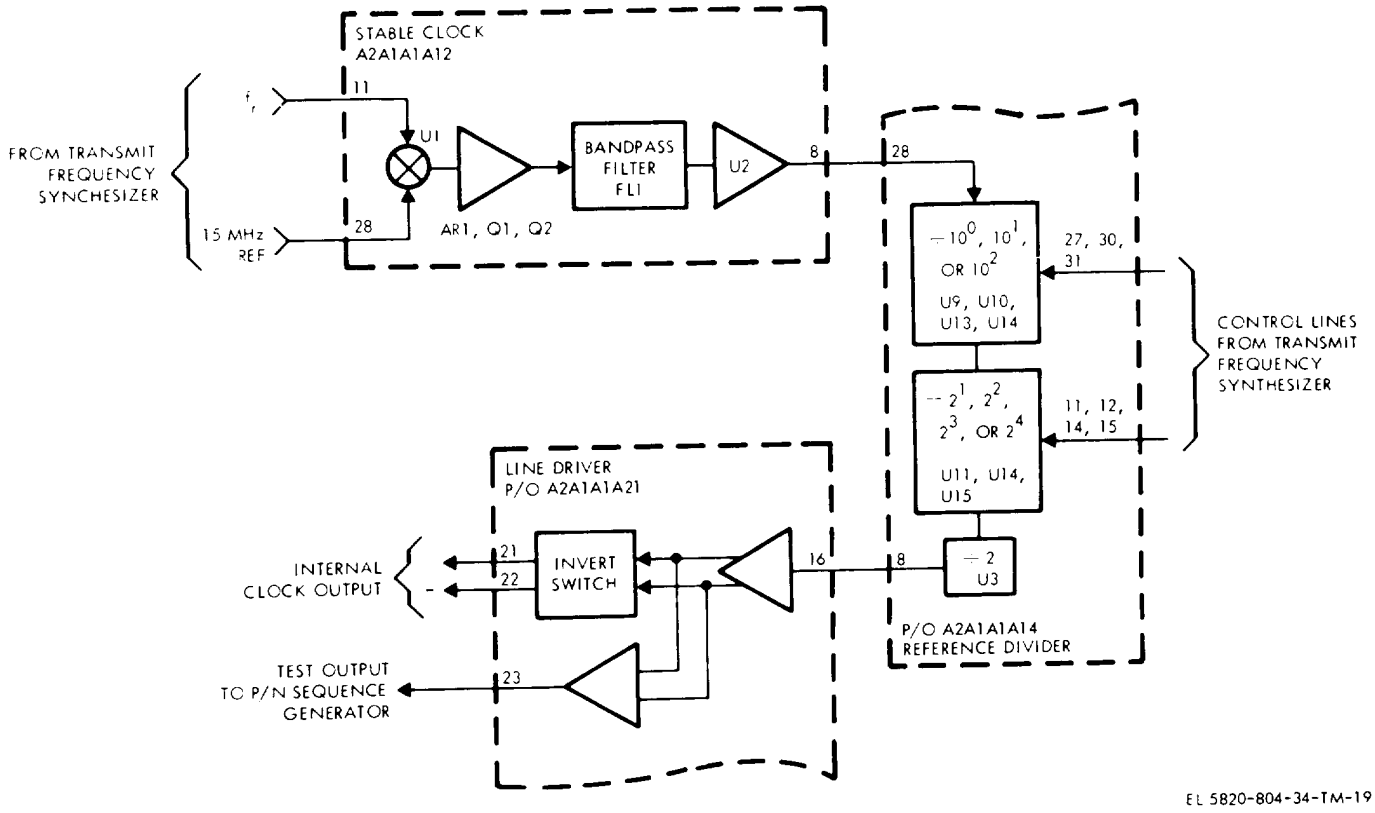

Figure 2-19. Internal clock generator, functional block diagram.

b. Stable Clock Circuit (fig. FO-21). The stable clock output is the selected bit rate, unaffected by variations in the control voltage to the VCO. To implement this function, the output of the 15 MHz reference oscillator is mixed with the amplified output of the 45 +10 MHz phase lock loop oscillator. The resultant 20-to-40-MHz clock is amplified, filtered, and then downcounted by decade and binary counters on an additional reference divider card.

(1) The 15-MHz input from the reference oscillator is received at the stable clock card via P1- 28 and applied across the attenuator formed by resistors R7, R11, and R12 to the input of mixer U1. The 45+10 MHz input from the 45-MHz amplifier is received via P1-11 and applied across the attenuator formed by R23 through R25 to the second input of the mixer. The difference frequency, 20 to 40 MHz, is transformer-coupled to the input of the three stage RF amplifier formed by operational amplifier AR1 and transistors Q1 and Q2. This amplifier is identical with the circuit used on the 45 MHz amplifier card and has a gain of approximately 40 to 56 dB as controlled by variable resistor R37.

(2) The output of transformer T2 is attenuated by R39, R41, and R42, and applied to low pass filter FLI. This filter suppresses undesired mixer products and provides an output through attenuator R40, R43, and R44 to ECL to TTL converter U2. The resultant stable output between 20 and 40 MHz is a multiple of the selected bit rate and is appropriately counted down to the selected frequency through binary and decade counters of the reference difider.

c. The operation of the reference divider is discussed in paragraph 2-5 d and the operation of the line driver is discussed in paragraph 2-12 b.

2-14. Test and Monitor Functions

a. General. The PSK modem contains a group of circuits which, in conjunction with various front panel indicators, provide a means of monitoring the operational status of the unit. The status monitoring capabilities along with the built-in test circuits provide a means of rapidly verifying operation or diagnosing a malfunction.

b. Fault and Status Monitor Functions. The signal flow of the fault and status monitor functions is shown in figure FO-2.

(1) The front panel fault indications are developed from the following signals:

(a) The transmit bit detector develops a logic 0 output when, in the transmit bit synchronizer, a loop filter overflow or underflow occurs (para 2-4 b and c).

(b) The transmit bit detector in the receive bit synchronizer develops a logic 0 output when a loop filter overflow or underflow occurs.

(c) The thermostat, which is positioned to monitor the temperature of the outlet air, provides a ground whenever the outlet air temperature exceeds 180°F.

(2) The presence of a fault indication other than overtemperature causes the same result. Each fault indication sets a latch circuit on the alarm circuits card. Each latch output is applied to one of two OR gates. One OR gate is activated by the transmitter section fault signal and the other by a receiver section fault signal. Each OR gate output illuminates a front panel indicator showing which section developed the fault signal. Additionally, the presence of a fault indication at either OR gate output causes the blinker generator and relay K1 (via driver U1) to be energized. Relay KI provides one contact closure for remote fault status monitoring purposes, and a second contact closure which activates the audible alarm if enabled by the front panel ALARM switch. The blinker generator output is gated with the latch outputs and the fault indicator signals to cause the appropriate front panel indicators to flash as long as the faults are present. If any of the faults are cleared after the appropriate latch circuits have been set, the gating networks provide steady ON indications at the front panel.

(3) The thermostat is connected directly to the associated indicator as well as the reset line and the audible alarm via a diode. In the event of a temperature fault, all fault indicators illuminate and the alarm sounds. In this case, none of the indications can be reset or disabled.

(4) All fault latches are resettable by momentarily setting the ALARM switch to RESET. The RESET position also illuminates all fault indicators for lamp test purposes.

(5) circuits on the digital to analog meter card are connected to monitor the data and clock inputs to the error comparator. The DATA and CLOCK indicators are located in the MONITOR section of the front panel. Each "A" indicator is illuminated when its input is a logic 1 and extinguished when its input is a logic 0.

(6) The front panel meter is controlled by the METER switch.

(a) With the METER switch in the OFF position, the meter is disconnected.

(b) In the +5 V, -6 V, +15V, and --15 V positions, the selected power supply voltages are applied to the meter through resistors on the alarm circuits card. The resistance associated with each voltage provides a meter input current of 100 μA, which results in a one-half scale deflection when nominal voltage is present.

(c) The 45-MHz phase lock loop cards in the transmit and receive frequency synthesizers each contain circuits which provide a nominal 100 μA output current into the meter when the loop is locked. When the loop is out of lock, the deviation from 100 AA is proportional to the difference between the programmable divider output frequency and the 400 Hz reference frequency (pare 2-5 e). These outputs are displayed on the meter when the METER switch is in the TX SYNTH and RX SYNTH positions.

(d) In the ERROR COUNT position of the METER switch, the meter displays the output of the D/A converter on the digital to analog meter card.
This indication is representative of the error comparator output. The METER switch also provides a ground output to the error comparator in this position.

(7) The error comparator receives data and clock inputs from various sections of the modem as selected by the SOURCE, METER, and TEST switches. The input clock drives a PN sequence generator identical to the one used to stimulate the test circuits. The input sequence is compared with the internally generated sequence and an output pulse is developed each time an input error occurs. The internal PN sequence generator may be synchronized to the input sequence by momentarily placing the MONITOR switch in the MANUAL position. When the MONITOR switch is in the AUTO position, the synchronization circuit is controlled by two counters. The bit counter monitors the input clock and divides the rate by 256. The error counter is preset to a count of 64 at the beginning of each bit counter cycle, and downcounts each time an error is detected. If the error counter downcounts to 0 before the bit counter resets it to 64 on the next

cycle, an output pulse is produced which resynchronizes the PN sequence generator.

(8) The digital to analog meter card produces an output current to the front panel meter based on the average input pulse rate. A clock loss detector circuit disables the input if a loss of clock should occur. An additional circuit monitors the bit and error counters to limit the number of error pulses gated to the D/A converter, and thus limits the meter drive current at high error rates.

c. Test Function. The test function provides for an internally generated pseudo-random data sequence to the ICF modem input circuits. The modem then reconstructs the input sequence. The data signals at various points in the modem are monitored as selected by front panel switch settings to deter- mine whether the proper sequence is present. A functional block diagram of the test circuits is shown in figure FO-3.

(1) The clock for the test function is taken from the test output of the line driver which provides the internally generated stable clock to the digital user (para 2-13). During normal operation, the SOURCE switch is in the OPERATE position and the PN sequence generator is disabled.

(2) When the SOURCE switch is in the LINK position, the PN sequence generator, which generates a 2047 bit sequence at the selected INPUT DATA RATE, is enabled and applied to the input circuits. The digital user inputs to the input circuits are also disabled by the SOURCE switch and the internally generated sequence is applied to the transmit bit synchronizer (para 2-3). As a result, the bipolar NRZ output is the internally generated PN sequence for link testing purposes.

(3) When the SOURCE switch is in the TEST position, the internal PN sequence generator is enabled and the sequence is applied to the transmit bit synchronizer as described above. If the TEST switch is in position 3 at this time, the PN sequence is also applied to the receive bit synchronizer through the NRZ interface card. Placing the SOURCE switch in the TEST position also accomplishes the following:

(a) The TEST switch, which controls the error comparator input in conjunction with the METER switch, is enabled.

(b) The relays on the LOS/cable receiver and decoder card and on the NRZ interface card are energized to disable the LOS/cable inputs and apply a test pattern from the drivers to the receive circuits (para 2-3).

(4) The data and clock inputs to the error comparator are selected according to the settings of the SOURCE and TEST switches which control the switching functions of the PN sequence generator card. When the SOURCE switch is in the OPER- ATE or LINK position, the standard data and clock test outputs are selected. When the SOURCE switch is in the TEST position, the error comparator inputs are selected by the TEST switch.

(a) In position 1, the PN sequence generator outputs are selected.

(b) In position 2, the transmit bit synchronizer outputs are selected.

(c) In position 3, the receive bit synchronizer outputs are selected.

(d) In position 4, the standard data and clock test outputs are selected.

(e) In position 5, the alternate data and clock outputs are selected.

(5) The PN sequence generator card provides an output pulse to the front panel synchronous with the 2047 bit pattern. A sample of the clock applied to the error comparator by the selection network is also provided to the front panel by the PN sequence generator card.

d. 11-Bit PNSequence Generator (Fig. FO-22).

(1) The PN sequence generator receives bit rate clock through gate U5 when P1-6 is high. P1-5 is connected externally to P1-45. P1-6 is low only when SOURCE switch is in OPERATE position, which disables the sequence generator. In LINK or TEST position, the generator is enabled. The sequence generator consists of two 8-bit shift registers, U7 and U8, the second and eleventh stages of which are exclusive OR'ed at Ull-6, gated with the output of the zero-suppression gate network, U10, U12, and U13, and fed back to the shift register in- put. The zero-suppression circuit prevents the generator from being locked up with all zeros. If all gates receive all ZERO inputs, a ONE is clocked into the register. The resulting sequence has a period of 2047 bits. The output is clocked through flip-flop U9 to pin 11. A negative sync pulse is provided at the front panel SYNC connector by detecting state 11100000000 using NAND gate U14.

(2) The clock and data selectors, U2 and U3, respectively, are controlled by their A, B, and C in- puts from OR gates U1 and U5. Pins 27, 62, 63, and 65 are set low by positions 1, 2, 3, and 5 of the TEST switch, respectively. Clock and data signals are ap- plied to the selectors from various internal test points in the modem. The complement outputs are applied to the error comparator via P1-17 and P1-25. The clock output is also provided to the front panel clock jack. The selected outputs determined by the TEST switch position are as shown in table 2-10.

(3) P1-9 and P1-10 are connected externally to allow flip-flop U9 to be used to divide the receive bit sync clock by 2. The flip-flop output is provided to the external decoder (para 2-11 b)

Table 2-10. Test Switch Selections

Position	Pin	Data	Pin	Clock
1	P1-59	Sequence generator clock	P1-51	Sequence generator output
2	P1-23	Transmit bit synchronizer clock	Pl-15	Transmit bit synchronizer output
3	Pl-58	Receive bit synchronizer clock	P1-50	Receive bit synchronizer sign bit output
4	P1-24	Standard clock test output via inverter U4 IPl-35)	Pl-16	Standard data test output
5	P1-19	Alternate clock test output via inverter U4 IPl-32)	P1-57	Alternate data test output

e. Error Comparator (fig. FO-23). The error comparator (A2A1A2A8) receives data and clock from the selector circuits on the 11-bit PN sequence generator card (A2A1A2A7).

(1) Shift registers, U1 and U2 along with exclusive OR U8 and gates U9 and U10 make up the PN sequence generator. The eleventh stage of the shift register (P1-6) is applied to P1-68 by an external connection. When the METER switch is in the ERROR COUNT Position, flip-flop U12 is preset by a ground on P1-30. Data and clock are applied to pins 32 and 25. In error count operation, U8-5 is high causing the complement data input to be inverted. The input data from U8-6 is compared with sequence generator data at exclusive OR gate U8 and the results applied to flip-flop U11-12. As long as the two data signals are identical, the output is low. If they are not the same, a high is generated which represents an error. The error signal at pin 51 is applied to the digital to analog meter card. The error pulses are also gated with clock, inverted by U7, and applied to the front panel ERROR jack for external counting.

(2) Binary counter U13 and U14 applies a reload input to downcounter U5 and U6 for every 256 clock pulses. A count equivalent to 64 counts is loaded by externally connected grounds on pin 22. The output of the 256 counter at pin 3 is also applied to the D/A meter circuit. When the error signal is high at AND gate U9-13, clock pulses are gated through to downcount U5 and U6. If there are 64 errors within 256 clock pulses, an overflow signal is generated by U6-13. This pulse at pin 23 is applied to the D/A meter card. Manual/automatic resynchronization of the sequence generator is controlled by gates U9 and U10 which are enabled by a low at either pin 50 or pin 52. Pin 50 is low when the MONITOR switch is in the AUTO position. U10-5 is therefore enabled, allowing the overflow pulse, which is externally connected to P1-24, to clear shift register U3 and U4 (P1-14 is externally connected to P1-36). The resultant low at U4-13 causes gates U9 and U 10 to load the input data into shift register U2. After 15 bits of input data have been loaded, U4-13 will go high again, since the shift register input is connected to a logic ONE, and the error comparator will revert back to normal operation. Placing the MONITOR switch in the MANUAL position places a ground on P1-52, which clears U3 and U4. When the switch is released, 15 bits of input data are loaded as described above.

f. Digital to Analog Meter (fig. FO-24). The digital to analog meter circuit (A2AlA2A9) converts the digital error data to an analog signal which is applied to the front panel MONITOR meter. In the condition of no error, pin 45 is low and OR gate U2-6 is high. Diodes CR1 and CR2 are forward biased applying a voltage which back-biases CR3, and no current is applied to the meter from P1-9. An error causes pin 45 to go high. Diode CR2 is back-biased and CR3 and CR4 are forward-biased, causing meter current flow. Capacitor C6 filters the current flow. The resultant meter deflection is proportional to the number of errors. Full scale deflection equals 25% error rate (64 errors in 256 clock pulses).

(1) Limit flip-flop U1 prevents the meter from deflecting beyond full scale. U1 is preset by count 256 at pin 44, placing U1-9 high. When overflow condition occurs (greater than 64 errors in 256 pulses), a positive pulse at pin 7 clocks a low to U1.
The low satisfies OR gate U2. The meter current flow is cut off until the next count 256 pulse.

(2) Clock pulses at pin 12 trigger retriggerable one-shot U3 thus keeping its output high. If clock pulses are lost, the one-shot output returns to a low. The low satisfies OR gate U5, thus cutting off meter current flow.

(3) The selected data and clock at pins 46 and 10, respectively, are applied to inverters and drivers.
The outputs drive the DATA A and B and the CLOCK A and B front panel indicators. Additionally, the operating voltages listed below are applied to the meter via this card:

Voltage	Input Pin	Output Pin
+5 V DC	47	11
-5 V DC	48	49
+15 V DC	15	52
-15 V DC	13	16

g. Alarm Circuits (fig. FO-25). The alarm circuits (A2A1A2A10) monitor the transmit and receive sections of the modem. In the event a fault occurs in the transmit bit synchronizer or the receive bit synchronizer, an alarm signal is generated. When a fault occurs, a high logic level is applied to the inverter of the apporpriate latching circuit. The output from the latching circuit activates a monostable multivibrator which produces a square wave output to the corresponding fault indicator on the front panel. This output causes the normally off indicator to blink on and off at approximately three times per second. In addition to the blinking indication, an audible alarm sounds. When the fault has been remedied, the indicator remains on until the ALARM switch is momentarily switched to the RESET position (the RESET posititon also acts as a lamp test for the indicators). The SECTION indicators illuminate when a fault occurs and remain on until reset, but they do not blink.

(1) The alarm circuits card contains six alarm detectors (only two are used). One detector, made up of inverter U3-4, latch U9-3 and 11, AND gate U10-3, OR gate U10-ll, and indicator driver U5-8, is discussed. The RESET signal sets all latches to test the front panel indicators. The low at U10-12 satisfies OR gate U10, thus keeping the indicator off when the RESET is released. When the associated fault occurs, pin 31 goes low. The low sets U9-3 low and U9-11 high. The low input from pin 31, inverted by U3, also enables AND gate U10-2. U10-1 receives a square wave signal from the flasher circuit. When the flasher input is high, U10-3 is low, flashing the indicator off. When the flasher input is low, U10-3 is high and the indicator is on. The low at U6-4 causes a low at pin 22, thus turning the RECEIVE section fault indicator on. The high at U6-6 activates alarm relay driver U1 and relay K1 energizes, causing the audible alarm to sound. If the low (fault) input should go high, the circuit will remain latched, but the low at U10-2 will disable the flasher input, keeping the indicator in the steady-on condition.

(2) The low at U7-3 also activates the flasher square wave generator, U11, U12 and associated circuitry. One-shot, U11, is initially triggered by this low. U11's Q output goes low, then returns high at the end of the one-shot operation. The return to high triggers one-shot U12. The Q output of U12, in turn, retriggers U11. This operation continues as long as the low at U11-1 or -2 remains. The square wave output from U11-8 is applied to AND gate U10-1 and the other fault circuits. The other alarm detect circuits operate the same although the circuits associated with P1-32, and P1-63 are activated by a high input.

CHAPTER 3

DIRECT SUPPORT MAINTENANCE INSTRUCTIONS

Section I. GENERAL

3-1. Scope of Direct Support Maintenance

This chapter contains detailed maintenance instructions to perform direct support maintenance on the ICF modem. Direct support maintenance includes all operator and organizational maintenance, plus troubleshooting, test, and replacement operations. A performance test is included to verify operability of the modem following repair (para 3-10). Do not go beyond the instructions given in this chapter.

3-2. DS Tools and Test Equipment

The equipment required for testing, troubleshooting, and repairing the ICF modem is listed below:

a. Oscilloscope, Tektronix 485A.
b. Digital Voltmeter, Fluke 8000A-01.
c. Tool Kit, Electronic Equipment TK-105/G.
d. Card Extenders, SM-D-759649 (2).
e. Card Puller, Protolab #7920.
f. Multimeter, VOM, Simpson 270.
g. Electronic Counter, HP 5245L with HP 5253 plug-in.
h. Oscilloscope Probe (X10), Tektronix 6054A (2). (Must use with TEK 485A.)

Section II. DIRECT SUPPORT TROUBLESHOOTING

3-3. General

Direct support maintenance personnel will, as required, perform the self-test procedures in this section to localize a fault. This procedures localizes a fault to several printed circuit cards or plug-in subassemblies. Direct support corrective action consists of interchanging those cards or subassemblies indicated to have possible faults with items known to be good. The items are interchanged one at a time in the order listed in each referenced corrective action table until the fault is corrected.

3-4. Troubleshooting Procedure

a. Perform the self-test procedure in accordance with paragraph 3-5. The self-test procedure defines a series of operations with corresponding requirements for resultant indications. If at any point in the self- test procedure the expected indication fails to occur, the appropriate corrective action is referenced.

b. Perform the corrective action in accordance with the portion of paragraph 3-6 that is referenced in the self-test procedure. When the corrective action appears to have corrected the fault indication, confirm operability be repeating the entire self-test procedure. If the corrective actions given in paragraph 3-6 fail to correct the faulty indication, refer to paragraph 3-7 to localize faults in the components which are not plug-in replaceable.

NOTE

Before any lengthy continuity tests are performed, the modem should be returned to its original condition and the troubleshooting procedure be repeated to be sure that malfunction indication did not result from operator error.

CAUTION

The modem covers must be in place for proper air flow to insure equipment cooling. If any maintenance operations require removal of cover(s) for extended periods (30 minutes or more), an external fan must be set up with air flow directly into the power supply area. Failure to observe this precaution will result in equipment damage.

c. After successful conclusion of self-test procedures following a corrective action, the modem may be returned to service immediately if required. To return the modem to service, refer to TM 11-5820-804-12 for the appropriate procedures. If operational requirements permit, perform the test in paragraph 3-10 to be sure the modem is operating within specification.

3-5. Self-Test Procedure

Refer to TM 11-5820-804-12 to determine the normal operational switch settings.

CAUTION

Performing self-test on a modem while the system is operating interrupts digital user communications on both the transmit and receive links.

a. Check to see that modem outputs to the data patch panel are properly terminated.

b. If modem is nonoperating, set the front panel switches as shown in table 3-1, set the POWER switch to ON, and allow 30 minutes for warmup.

Table 3-1. Self-Test Initial Switch Settings

Control section	Switch	Position
FAULT	ALARM	OFF
TRANSMIT	INPUT DATA RATE	Same as operational INPUT DATA RATE
	ERROR CODING	NONE
	SOURCE	TEST
MONITOR	TEST	1
	METER	OFF
	MANUAL/OFF/AUTO	AUTO
RECEIVE	SYMBOL RATE	Same as operational INPUT DATA RATE
	ERROR CODING	NONE
	ON/OFF	ON
	STD/CLK/ICF	Same as operational setting
Behind upper front panel	DIFF ENCODE	ON
	DIFF DECODE	ON

c. If modem is in operation, initiate the test by changing the modem switch settings as required to correspond to table 3-1.

d. Connect the electronic counter to the modem front panel ERROR jack.

e. Perform the self-test in accordance with table 3-2 and the following instructions:

(1) In the sequence shown on the table, set each front panel switch indicated in the first column to the corresponding setting (s) indicated in the second column.

(2) For each switch setting, observe the indicator (s) listed in the third column, and verify the results required by the fourth column.

f. If operational INPUT DATA RATE is not the same as operational SYMBOL RATE, set both switch groups to the operational SYMBOL RATE and repeat procedures of table 3-2.

Table 3-2. Self-Test Procedure

Control section) switch	Setting	Indicator	Normal Indication	Corrective action
		POWER ON	Illuminated	Table 3-4
(FAULT) ALARM	Hold in RESET	ALL FAULT indicators	Illuminated	Table 3-5
		Audible ALARM	Tone	Table 3-5
(FAULT) ALARM	Release to OFF	Audible ALARM	No tone	Table 3-6
		TEMPERATURE	Extinguished	Table 3-6
(MONITOR) METER	+5	Meter	46 to 54	Table 3-7
	-5 Meter	46 to 54	Table 3-7	
	+ 15	Meter	46 to 54	Table 3-7
	--15	Meter	46 to 54	Table 3-7
	XMIT SYNTH	Meter	40 to 60	Table 3-8
	RCV SYNTH ERROR COUNT	Meter	40 to 60	Table 3-9
(MONITOR) TEST	1	Meter and electronic counter	0	Table 3-10
		ALL MONITOR indicators	Illuminated	Table 3-10
	2	Same as above	No change	Table 3-11
	3	Same as above	No change	Table 3-12
	4	Same as above	No change	Table 3-13
	5	Same as above	No change	Table 3-14
(FAULT) ALARM	RESET (momentary)	ALL FAULT indicators	Extinguished	Table 3-15

g. Set the DIFF ENCODE or DIFF DECODE switch to ON, and verify that MONITOR meter indicates 0 and that DATA and CLOCK indicators are illuminated. (For corrective action, refer to table 3-16.).

h. If both ERROR CODING switches are operationally set to NONE omit procedures of table 3-3.

i. If the RECEIVE ERROR CODING switch is operationally set to EXTERNAL, set both ERROR CODING switches to that position, set SYMBOL RATE switches to operational positions, and set INPUT DATA RATE switches to one-half the operational SYMBOL RATE. Then perform the coder test in accordance with table 3-3.

j. If the TRANSMIT ERROR CODING switch is operationally set to EXTERNAL, set both ERROR CODING switches to that position, set INPUT DATA RATE switches to operational positions, and set SYMBOL RATE switches to twice the INPUT DATA RATE. Then perform (or repeat) the coder test in accordance with table 3-3.

Table 3-3. Coder/Decoder Test Procedure

(Control section) switch	Setting	Indicator	Normal Indication	Corrective action
(MONITOR) TEST	5			
(MONITOR) METER	ERROR COUNT	Meter and electronic counter	0	Table 3-17
		ALL MONITOR indicators	Illuminated	Table 3-17
FAULT ALARM	RESET (monentary)	AI,L FAULT indicators	Extinguished	Table 3-17

3-6. Corrective Action

The follwoing corrective action procedure provides a means of isolating a failed subassembly and repairing the modem. Tables 3-4 through 3-17 contain the fault isolation procedures to be sued in the event of a self-test failure. Table 3-18 lists the alinement or adjustment procedures required after replacement of certain subassemblies.

a. Perform any additional observations or tests required by the table and use this information to select the required corrective actions.

b. Perform the corrective actions in the sequence given, and monitor the unit to determine whether the corrective action clears the fault. For example, if the corrective action column lists several potentially faulty PC cards, replace the first card listed. If the fault indication status of the modem remains unchanged, return the original card to the modem, and then replace the second card on the list. Continue in this sequence until the fault is cleared.

c. When a corrective action is performed which apparently clears the faulty indication, confirm the repair by rerunning the self-test (para 3-5).

d. The replacement of several subassemblies of the ICF modem requires that alinement or adjustment be performed. The specific procedures of alinement and adjustment of these subassemblies (which are indicated by a single asterisk (*) in the corrective action columns) are referenced from table 3-18.

e. If any of the cards which contain switches are replaced to repair a fault, the switches on the replacement card must be set properly to interface with the system. The cards which contain switches are indicated in the corrective action columns by a double asterisk (**). Set the switches on the replacement cards the same as the switches on the card to be removed. Detailed information on the required switch settings is contained in TM 11-5820- 804-12.

Table 3-4. Fault Isolation Procedure, (POWER Indicator)

Symptom	Corrective action	Notes
POWER indicator extinguished	1.1If the fuse indicator is illuminated, perform procedures below If extinguished. proceed to step 2 a Set POWER switch to off b. Disconnect connector A2PI from power supply c. Replace A1FO1. d. Set POWER switch to ON and verify fuse indicator is extinguished.	Fuse

Table 3-4. Fault Isolation Procedure (POWER Indicator)-Continued

Symptom	Corrective action	Notes
	e. Set POWER switch to off and reconnect A2P1 to power supply.	
	f. Set POWER switch to ON and verify fuse indicator if extinguished. If the fuse indicator again illuminates, replace power supply A2PSI* and AlFO1.	
	2. If other front panel indicators are illuminated, replace indicator A1DS11.	POWER indicator lamp
	3 Check ac line cord and POWER ON/off switch and repair or replace if required.	

Table 3-5. Fault Isolation Procedure (ALARM RESET)

Symptom	Corrective action	Notes
One or more FAULT indicators extinguished	1. If no FAULT indicators are illuminated proceed to step 2. If other indicators are illuminated, perform a and b. below.	
	a. Replace faulty indicator bulb.	
	b. Replace A2A1A2A10.	Alarm circuits (SM-D-742033)
	2. Operate METER switch to +5 V position. If meter reading is less than 46 replace A2PS1*.	Power supply
	3. Check ALARM switch, A1S1, and replace if required.	RESET position
No audible alarm	Replace:	
	a. A2AlA2A10	Alarm circuits (SM-D-742033)
	b. AIDS1	Audible alarm

Table 3-6. Fault Isolation Procedure (ALARM OFF)

Symptom	Corrective action	Notes
Audible alarm tone or TEMPERATURE indicator on	Replace:	
	a. A2AlA2A10	Alarm circuits (SM-D-7420331
	b. A2S1	Thermostat

Table 3-7. Fault Isolation Procedure (Power Supply)

Symptom	Corrective action	Notes
Meter indication out of limits	Replace’	
	a. A2PS1*	Power supply (SM-C-742003)
	b. A2AlA2A9	D/A meter (SM-D-7420651
	c. A1M1	Meter

Table 3-8. Fault Isolation Procedure (XMIT SYNTH)

Symptom	Corrective action	Notes
Meter indication not within limits (40 to 60)	Replace :	Wait approximately 15 seconds for proper indication after each replacement.
	a. A2A1A1A6*	45 MHz PLL (SM-D-742113)
	b. A2AlA1A3*	Reference oscillator (SM-D-742129)
	c. A2AlAlAA	Counter encoder (SM-D-742105)
	d. A2A1AlA2	Prog. divider (SM-D-742109)
	e. A2A1A1A5	Reference divider (SM-D-742133)
	f. A2A1A1A8*	45 MHz amp (SM-D-742117)
	g. A1A1	INPUT DATA RATE switches

Table 3-9. Fault Isolation Procedure (RCV SYNTH)

Symptom	Corrective action	Notes
Meter indication not within limits (40 to 60)	Replace:	Wait approximately 15 seconds for proper indication after each replacement
	a. A2A1A2A18*	45 MHz PLL (SM-D-742113)
	b. A2A1A2A21*	Reference oscillator (SM-D-742129)
	c. A2A1A2A24	Counter encoder (SM-D-742105)
	d. A2A1A2A23	Prog. divider ISM-D-742109)
	e. A2A1A2A20	Reference divider (SM-D-742133)
	f. A2A1A2A16*	45 MHz amp (SM-D-742117)
	g. A1A2	SYMBOL RATE switches

Table 3-10. Fault Isolation Procedure (TEST 1)

Symptom	Corrective action	Notes
Clock A or B extinguished	Replace:	
	a. A2A1AIA12*	Stable clock iSM-D-731201)
	b. A2A1A1A3*	Reference oscillator (SM-D-742129)
	c. A2A1A1A14	Reference divider (SM-D-742133)
	d. A2AIA1A21**	Line driver (SM-D-742053)
	e. A2A1A2A7	PN sequence generator (SM-D-742057)
	f. A2A1A2A9	D/A meter (SM-D-742065)
	g. CLOCK A or B indicator	
DATA A or B extinguished	Replace:	
	a. A2A1A2A7	PN sequence generator (SM-D-742057)
	b. A2A1A2A9	D/A meter {SM-D-742065)
	c. DATA A or B indicator	
Meter indication other than 0	Replace:	
	a. A2A1A2A7	PN sequence generator ISM-D-742057)
	b. A2A1A2A8	Error comparator (SM-D-742061)
	c. A2A1A2A9	D/A meter (SM-D-742065)
	d. A2A1A2A4**	Input interface (SM-D-742037)

Table 3-11. Fault Isolation Procedure (TEST 2)

Symptom	Corrective action	Notes
CLOCK A or B extinguished	Replace:	
	a. A2A1A1A3*	Reference oscillator {SM-D-7421291
	b. A2A1A1A5	Reference divider (SM-D-742133)
	c. A2A1A1A10*	Mixer/output amp (SM-D-742125)
	d. A2A1A1All	15 MHz amp (SM-D-742121)
	e. A2A1A1A17	Transmit bit detector (SM-D-742045)
	f. A2Y2*	VCO (SM-A-731369-1)
DATA A or B extinguished	Replace:	
	a. A2A1A2A4**	Input interface (SM-D-742037)
	b. A2A1A1A17	Transmit bit detector (SM-D-742045)
Meter indication other than 0	1. Replace:	
	a. A2A1A1A15	D/A converter (SM-D-731217)
	b. A2A1A1A16	Loop filter (SM-D-731221)
	c. A2A1AIA17	Transmit bit detector (SM-D-742045)
	2. Replace cards listed above for CLOCK A or B extinguished symptom.	

Table 3-12. Fault Isolation Procedure (TEST 3)

Symptom	Corrective action	Notes
CLOCK A or B extinguished	Replace:	
	a. A2AlA2A15*	Mixer/output amp (SM-D-742125)
	b. A2A1A2A14	15 MHz amp (SM-D-742121)
	c. A2AlA2A20	Reference divider (SM-D-742133)
	d. A2A1A2All	Transmit bit detector (SM-D-742045)
	e. A2A1A2A21*	Reference oscillator (SM-D-742129)
	f. A2Y1*	VCO (SM-A-731369-1)
DATA A or B extinguished	Replace:	
	a. A2A1A2A5	Coder interface (SM-D-742049)
	b. A2A1A2A6	Coder switch (SM-D-742041)
	c. A2A1A2All	Transmit bit detector (SM-D-742045)
	d. A2A1A2A2	NRZ interface (SM-D-877791)
Meter indication other than 0	1. Replace:	
	a. A2A1A2A13	D/A converter (SM-D-731217)
	b. A2A1A2A12	Loop filter (SM-D-731221)
	c. A2A1A2A14	15 MHz amp (SM-D-742121)
	2. Replace cards listed above for CLOCK A or B extinguished symptom	
	3. Replace A2Y1*	VCO (SM-A-731369-1)

Table 3-13. Fault Isolation Procedure (TEST 4)

Symptom	Corrective action	Notes
CLOCK A or B extinguished, Data A or B extinguished, or meter indication other than 0.	Replace:	
	a. A2A1A2A3	LOS/cable driver (SM-D-742081)
	b. A2AlA2A1	LOS/cable receiver and decoder (SM -D-742089)
	c. A2A1A2A4**	Input interface (SM-D-742037)
	d. A2A1A2A23**	Standard line driver (SM-D-742053)
	e. A2A1A2A6	Coder switch (SM-D-742041)
	f. A2A1A2A2	NRZ interface (SM-D-877791)

Table 3-14. Fault Isolation Procedure (TEST 5)

Symptom	Corrective action	Notes
DATA A or B or CLOCK A or B extinguished or meter indication other than 0.	Replace A2A1AlA22**	Alternate line driver (SM-D-742053)

Table 3-15. Fault Isolation Procedure (DIFF (Momentary RESET))

Symptom	Corrective action	Notes
Any FAULT indicator illuminated or blinking	Replace A2AlA2A10	Alarm circuits (SM-D-742033)
TRANSMIT BIT SYNC illuminated or blinking	Replace A2A1A1A17	Transmit bit detector (SM -D-742045)
RECEIVE BIT SYNC illuminated or blinking	Replace A2A1A2All	Transmit bit detector (SM -D-742045)

Table 3-16. Fault Isolation Procedure (DIFF ENCODE/DECODE)

Symptom	Corrective action	Notes
Any improper indication	Replace A2A1A2A6	Coder switch (SM-D-742041)

Table 3-17. Fault Isolation Procedure (Coder/Decoder Test D

Symptom	Corrective action	Notes
Any improper indication (external error coding)	Replace:	
	a. A2A1A2A5**	Coder interface (SM-D-742049)
	b. A2A1A2A6	Coder switch (SM-D-742041)

Table 3-18. Alinement and Adjustment Following Repair Action

Subassembly	Alinement adjustment requirements
A2AIA2A1 (I,OS/cable receiver and decoder	Perform the LOS/cable receiver alinement in accordance with paragraph 2-18. TM 11-5820-804-12.
A2AI1AI A3 and A2A1A2A21 (Reference oscillator)	Perform the frequency synthesizer alinement (para 3-8 c).
A2AIAIA6 and A2AIA2A18 (45 MHz PLL)	Perform the frequency synthesizer alinement (para 3-8 c).
A2AIAIA8 and A2A1A2A16 (45 MHz amplifier)	Perform the frequency synthesizer alinement (para 3-8 c).
A2AIAIA10 and A2A1A2A15 (Mixer/output amplifier)	Perform the frequency synthesizer alinement (para 3-8 c).
A2AIAIA12 (stable clock)	Perform the frequency synthesizer alinement (para 3-8 c).
A2PS1 (Power supply)	Perform the power supply adjustment in accordance with paragraph 5-9, TM 11-5820-804-12.
A2YI (Oscillator)	Perform the oscillator adjustment (para 3-8 b I.
A2Y2 (Oscillator)	Same as A2Y1.

3-7. Chassis and Card File Fault Isolation

a. General. This paragraph contains the fault isolation information for ICF Modem components that are not plug-in replaceable.

b. Card Files. If the fault is not corrected by the substitution method of troubleshooting, continutiy checks between connectors must be made. Refer to table B-1 and perform continuity tests in the suspect area.

c. Chassis Wiring. Continuity tests are made between external connectors and points in the modem or between internal points within the modem. Refer to figure FO-26. Table 3-19 gives a list and description of the connectors.

Table 3-19. ICF Modem Connectors

Designation	Type	Description
A1J1	External	Error test point
A1A2	External	Sync test point
A1IJ3	External	Clock test point
A2J4	External	Ac power to the rack
A2J5	External	Digital user interface with modem
A2J6	External	Coder decoder Interface with modem
A2E2	External	Static ground
A2E5	External	Single point ground
AIPI A2PSIJI	Internal	Ac power
AIA2POI A2AIA1J3	Internal	Switch assembly to cardfile
AIP02 A2A1AIJ2	Internal	Lights and switches from motherboard to front panel
A1PO3/A2A1A1J1	Internal	Switches and test jacks from motherboard to front panel
A1A1PO1/A2A1A2J1	Internal	Switch assembly to cardfile
A2W09-1/A2A1W1-1	Internal	Ground return
A2W9-2/A2E5-B	Internal	Ground return
A2W 11P1/ A2A1J2	Internal	Oscillator cable
A2WV 11 P2 A2Y1J1	Internal	Oscillator cable
A2W11 P3/A2Y2J1	Internal	Oscillator cable

Section III. DIRECT SUPPORT ALINEMENT AND REPAIR

3-8. Adjustment and Alinement Procedure

a. General. The procedures required to adjust the oscillators and frequency synthesizer to obtain optimum performance are contained in this paragraph. Refer to TM 11-5820-804-12 to determine the normal operational switch settings

b. Oscillator Adjustment Procedure. An oscilloscope, card extender, and card puller are required for oscillator adjustment.

NOTE

Oscillator circuits A2Y1 and A2Y2 are contained in internal ovens. The required oven stabilization time is 30 minutes prior to adjustment.

(1) Set the ICF modem front panel controls as shown in table 3-20.

(2) Set the POWER switch to the off position and disconnect both oscillators from the mounting and retaining brackets to provide access to the appropriate adjustment (access opening is located on the oscillator surface oppostie the connector).

(3) If A2Y2 is to be adjusted, remove card A2A1A1A11, insert the card extender in the card slot, and insert A2A1A1A11 into the card extender. If A2Y1 is to be adjusted, place A2A1A2A14 on the extender card.

Table 3-20. Initial Control Settings for Oscillator Adjustments

Control	Position
ALARM	OFF
TRANSMIT SOURCE	TEST
TRANSMIT ERROR CODING	NONE
INPUT DATA RATE	Same as operational SYMBOL RATE switch settings
DIFF ENCODE	ON
DIFF DECODE	ON
SYMBOL RATE	Same as operational SYMBOL RATE switch settings
RECEIVE ERROR CODING	NONE

(4) Set the POWER switch to ON position. Connect oscilloscope to observe the signal on pin 21 of the extended card and adjust the oscillator to produce a waveform centered at 0 volt.

(5) Set POWER switch to off, remove card extender, and replace extended card.

c. Frequency Synthesizer Alinement. A frequency counter, an oscilloscope, two card ex- tenders, and a card puller are required to aline the frequency synthesizer.

NOTE

The following procedures are used to aline either the transmit or the receive frequency synthesizer. The receive frequency synthesizer reference designators are shown in parenthesis. If any adjustment fails to result in the specified indication, the probable cause is failure of the card being adjusted. If the measurement is taken from a card other than that which is adjusted, the next most probable cause is failure of the card from which the measurement is taken.

(1) Set front panel SOURCE switch to TEST and, with power removed, place reference oscillator card A2A1A1A3 (A2A1A2A21) on a card extender. Also place 45 MHz amplifier card A2A1A1A8 (A2A1A2A16) on an extender card. Apply power and connect frequency counter to monitor output pin 21 on reference oscillator. As required, adjust 15 MHz TCXO Y1 on reference oscillator (fig. 3-1) for a frequency counter indication of 15 MHz +2 Hz.

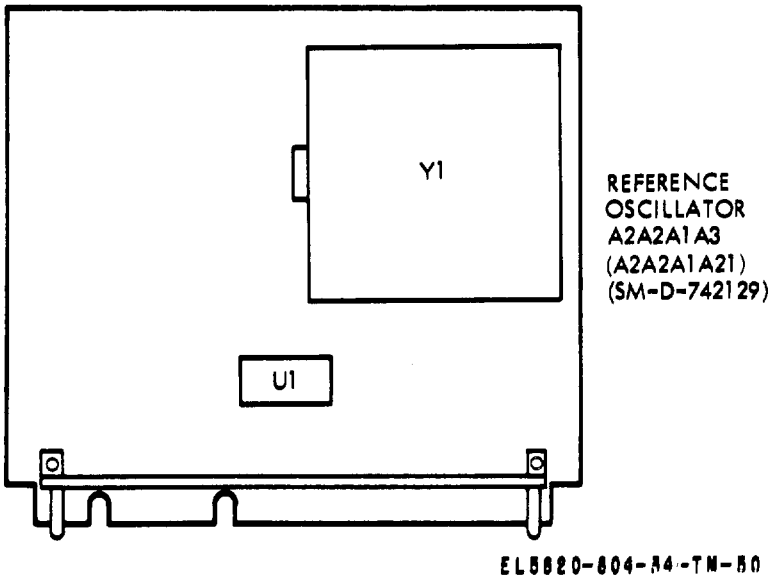

Figure 3-1. Reference oscillator adjustment location.

(2) Set front panel INPUT DATA RATE (SYMBOL RATE) thumbwheel switches to 9.9999 MB/S. Connect oscilloscope to monitor amplitude at pin 22 of 45 MHz amplifier card. Continue to monitor amplitude at pin 22 and set INPUT DATA RATE ISYMBOL RATE) thumbwheel switches to 56.0000 MB/S.

(3) Amplitude at pin 22 should be 2,0 : 0,1 volts p.p. As required, adjust R24 (fig. 3-2) to obtain best indication (as close to 2.0 volts p-p as possible) at both rates (9,9999MB/S and 5.0000 MB/S)

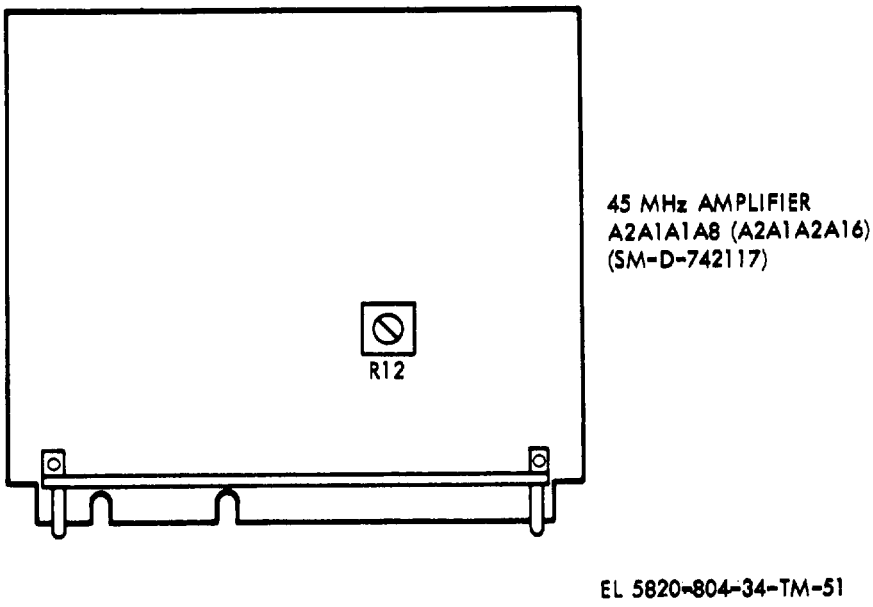

Figure 3-2. 45 MHz amplifier adjustment location.

(4) Set front panel thumbwheel switches to 9.9999 MB/S. Connect oscilloscope to monitor signal amplitude at pin 1 of circuit U1 (fig. 3-1) on the reference oscillator card. Continue to monitor amplitude at U1-1 and set thumbwheel switches to 5.0000 MB/S.

(5) Amplitude at Ul-1 should be 0.5 -0.005 volt p-p at both rates of (4) above. If amplitude is not as specified, remove power and remove 45 MHz amplifier from the extender. Return 45 MHz amplifier to its proper position in the file and place mixer/output amplifier A2A1A1A10 (A2AlA2A15) on the extender. Apply power and, as required, adjust R33 (fig. 3-3) on the mixer/output amplifier to obtain best indication (as close to 0.5 volt p-p as possible) at both rates (9.9999 MB/S and 5.0000 MB/S).

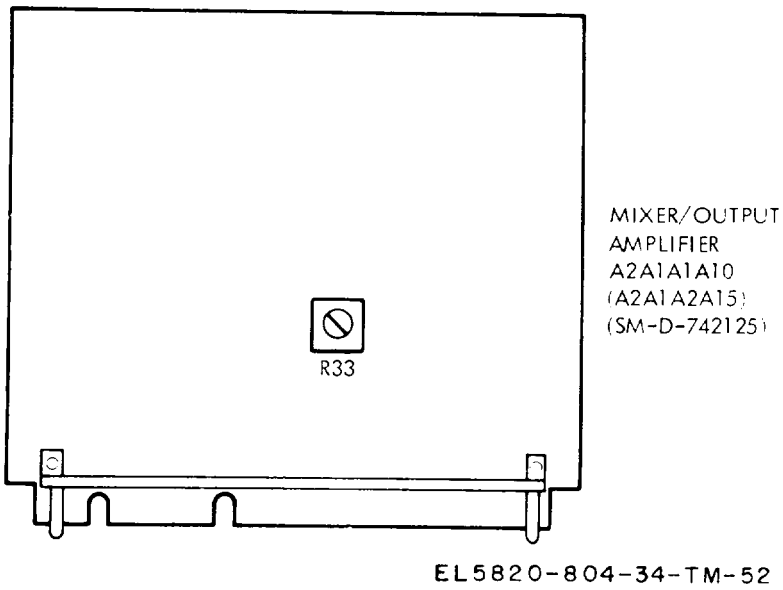

Figure 3-3. Mixer output amplifier adjustment location

(6) Remove power and remove card extender (s). Return circuit card is) to their proper positions in the file. Place 45 MHz phase lock loop card A2A1A1A6 (A2A1A2A18) on an extender. If alining the transmit synthesizer, place stable clock card A2AlA1A12 on an extender. Apply power.

(7) Set thumbwheel switches to 7.5000 MB/S. Connect oscilloscope to pin 4 of oscillator U1 (fig. 3- 4) on the 45 MHz phase lock loop card. As required, adjust oscillator Y1 so that with the loop locked the oscilloscope indication is 0 +0.1 volt.

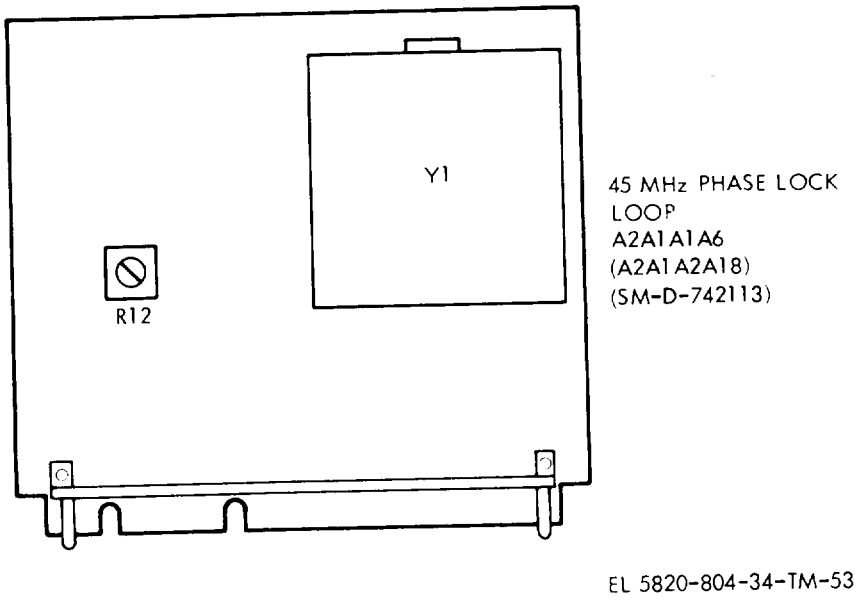

Figure 3-4. 45 MHz phase lock loop adjustment locations

(8) On front panel MONITOR section, set METER switch to XMT SYNTH (RCV SYNTH). On 45 MHz phase lock loop card, adjust R12 to ,obtain a front panel meter indication of 50 +2.

(9) If alining the transmit synthesizer, connect oscilloscope to monitor amplitude at pin 9 of U2 (fig. 3-5) on stable clock card A2A1A1A12. As required, adjust R37 on this card to obtain an oscilloscope indication of 0.5 -0.05 volt p-p. If adjustment is necessary, repeat (7) and (8) above after completing this adjustment.

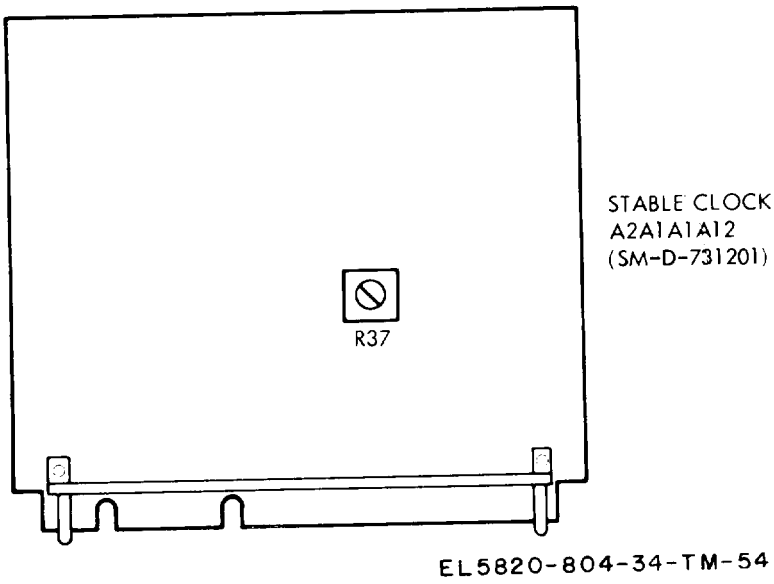

Figure 3-5. Stable clock adjustment location.

(10) Remove power and remove card extenders. Return 45 MHz phase lock loop card (and stable clock card if previously extended) to proper position in card file. Place 16 MHz amplifier A2A1A1A11 (A2A1A2A14) on an extender. Apply power.

(11) Connect oscilloscope to monitor amplitude at pin 21 of the 15 MHz amplifier and adjust A2Y2 (A2Y1) as required to obtain an oscilloscope indication of 0 : K0.06 volt.

(12) Remove card extender and return 15 MHz amplifier to its proper position in the card file.

(13) If completing alinement of the transmit synthesizer, connect frequency counter to monitor output of front panel CLOCK connector. Set TEST switch to position 1 and exercise INPUT DATA RATE switches through each position and verify counter indicates selected frequency $\pm$1 least significant digit.

(14) If completing alinement of the receive synthesizer, connect frequency counter to monitor output of front panel CLOCK connector. Set TEST switch to position 3 and exercise SYMBOL RATE switches through each position and verify counter indicates selected frequency $\pm$1 least significant digit.

3-9. Removal and Replacement Procedures

a. General. Removal and replacement of most subassemblies is obvious by inspection. However, the power supply has much attaching hardware and the following procedures will aid in its removal and replacement.

b. Power Supply.

(1) With modem top cover removed, disconnect the ac power cable PS1J1 and the dc connector to the top file. Remove four Phillip's-head screws (A, fig. 3-6). With modem bottom cover removed, remove two lower Phillip's-head screws from each side near bottom of the omdem (B, fig. 3-6). Extract power supply with attached mounting brackets from bottom of modem.

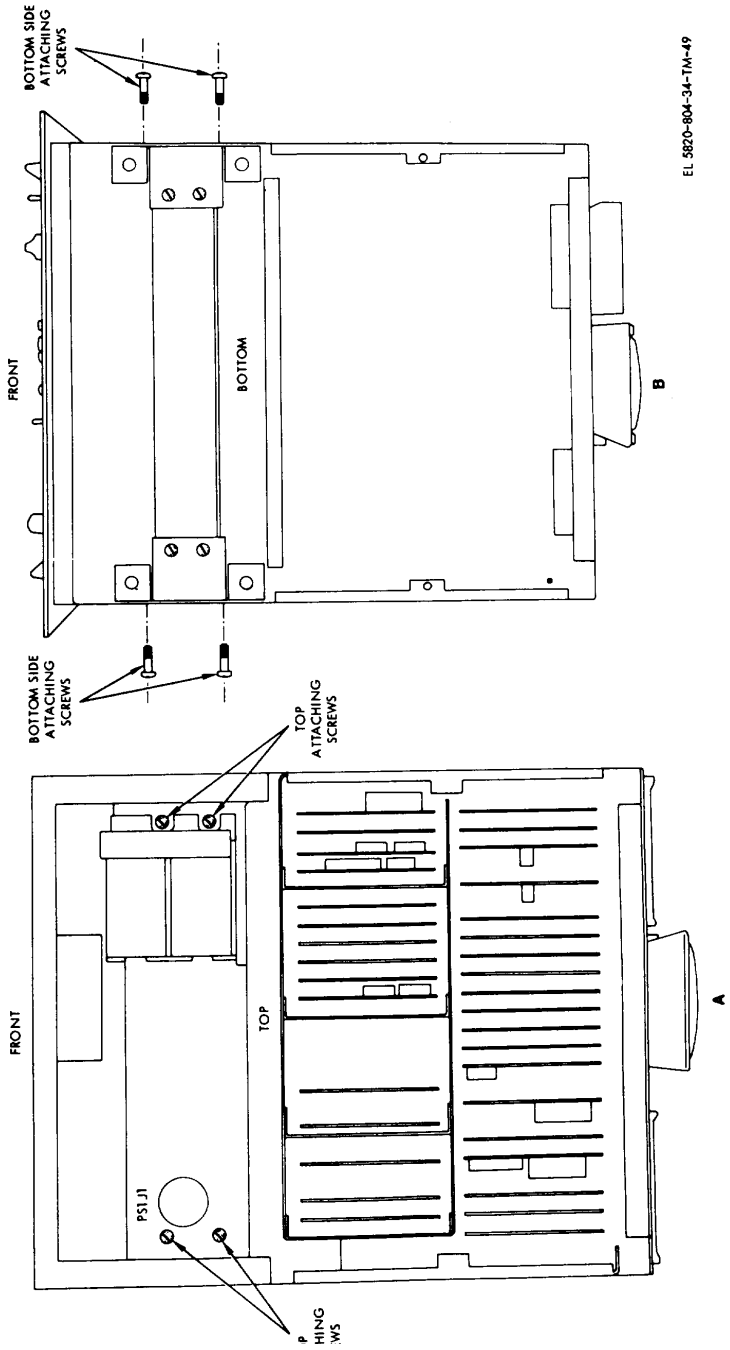

Figure 3-6. Power supply removal and replacement.

(2) If replacing the supply, remove the power supply mounting brackets and install brackets on replacement supply (replacement supplies are not provided with mounting brackets.

(3) To reinstall the supply. reverse the procedures of (1) above. Leave screws untightened and ensure that the mounting brackets are flush with the bottom sides of the modem; then tighten screws.

3-10. Performance Testing

Performance verification of the ICF modem is accomplished through restoring the ICF modem to its operational configuration and performance of link test. Refer to TM 11-5820-804-12.

GENERAL SUPPORT MAINTENANCE INSTRUCTIONS (OR SELECTED REPAIR ACTIVITY (SRA))

4-1 . Scope of General Support Maintenance and Selected Repair Activity (SRA) Maintenance

General support maintenance and selected repair activity (SRA) consists of testing, adjusting, and repairing all repairable assemblies of the ICF modem. Procedures for ICF modem, subassembly (card) tests, adjustment, and repair are provided in DMWR 11-5820-804.

4-2 . Tools and Test Equipment

GS and SRA tools and test equipment are listed below.

a AC Voltmeter, HP 400F.
b Attenuator Fixture SM-D-877511 (2 required).
c Automatic Test System, GR-1792.
d Autotransformer, Variac W50M.
e Digital Voltmeter, Fluke 8000A-01.
f Electronic Counter, HP 5245L with HP 5253 (2 required).
g Error Rate Counter TS-3641/G (Harris 7002).
h Function Generator, Wavetek 142.
i Multimeter, Simpson 270.
j Oscilloscope, Tektronix 485A.
k Oscilloscope Probe, X10; Tektronix P6054A (2 required).
1 Power Meter, Millivac MV 828B.
m Power Supply Test Set, ICF modem, SM- C-742003.
n Precision Power Supply, Power Design 4010.
o Pulse Generator, Datapulse 11OB (2 required).
p Resistor Decade Box, General Radio GR 1434M.
q Signal Generator, HP 606B.
r Signal Generator, HP 608F.
s Spectrum Analyzer, HP 141T with Plug-Ins HP 8552B and HP 8553B.
t Sweep Generator, HP 8601A.
u Synchronizer, HP 8708A.
v Termination: 50-ohm feed-thru, Tektronix 011-0049-01 (2 required).
w Termination: 50-ohm, Amphenol 35725-51 (2 required).
x Test Set, ACDC Co. Model 66-991-000.
y Card Extender SM-D-759649 (2 required).
z Card Test Fixtures (Harris T-14301 thru T-14306):
(1) SM-D-868407.
(2) SM-D-868408.
(3) SM-D-868410.
(4) SM-D-868412.
(5) SM-D-868414.
(6) SM-D-868416.
aa Card Puller, Protolab 7920.
ab Digital Card Test Adapter, SM-D-868405 (Harris T14146).
ac Interface Test Unit, SM-D-877812 (Harris T-14397).
ad Pin Crimp Tool and Turret, MS22520-1-01 and MS22520-1-02.
ae Pin extraction tools:
af MS24256R16.
(1) MS24256R20.
(2) Teradyne 600-0027-000.
(3) Burndy RX 20-25.
ag Pin insertion tools:
(1) MS24256A16.
(2) MS24256A20.
ah Power Supply Fixture SM-D-868418.
ai Tool Kit, Electronic Equipment TK-105/G.
aj Power Supply/Oscillator Test Fixture, SM-D-882197.
ak Resistors, 2 watts: 36, 50, and 75 ohms.

CHAPTER 5
ICF MODEM POWER SUPPLY DESCRIPTION AND MAINTENANCE INSTRUCTIONS

Section I. GENERAL DESCRIPTION

5-1. Scope

This chapter contains descriptive information and maintenance procedures for power supply PS1, which provides all the dc power requirements for the ICF modem. This section describes the physical and electrical characteristics and identifies the constituent subassemblies of the power supply. Section II gives a detailed explanation of circuit operation. Direct support troubleshooting and maintenance instructions are provided in section III.

5-2. Physical Characteristics

The power supply (fig. 5-1) is physically comprised of a metal chassis that contains most of the electronics, and three heat-sink assemblies that are attached to one side of the metal chassis. The dimensions of the metal chassis are 8 x 15 x 2.5 inches, and the complete assembly, including the heat sinks, weighs 16 pounds. Input power to the supply is furnished through an external cable that connects to chassis-mounted jack J1 (fig. 5-2). Outputs from the power supply are routed through a single cable, approximately 20 inches long, and terminated in plug P1. The output plug connects to jack A2A1J1 located on the side of the ICF modem card file. External test points are provided on the power supply for monitoring the dc outputs, and access ports are available to allow screwdriver adjustment of individual out-put voltages. The 10 major subassemblies (fig. 5-1 and 5-2) of the power supply are listed below with their associated reference designators. Figure 5-1. Power supply PS1, external view.

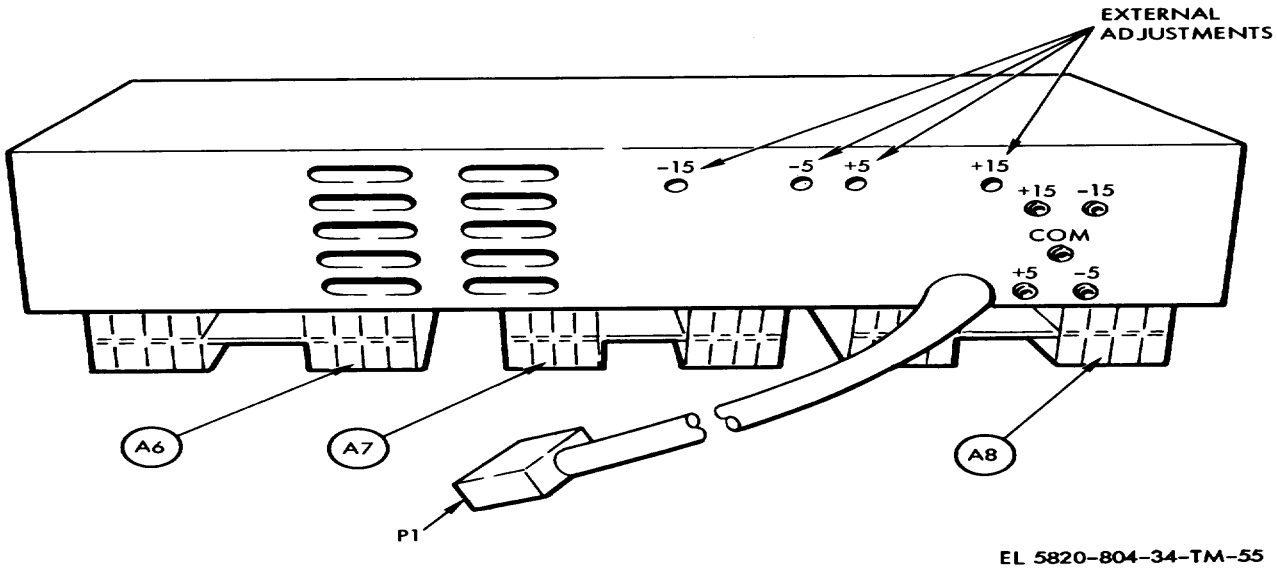

Figure 5-1. Power supply PS1, external view.

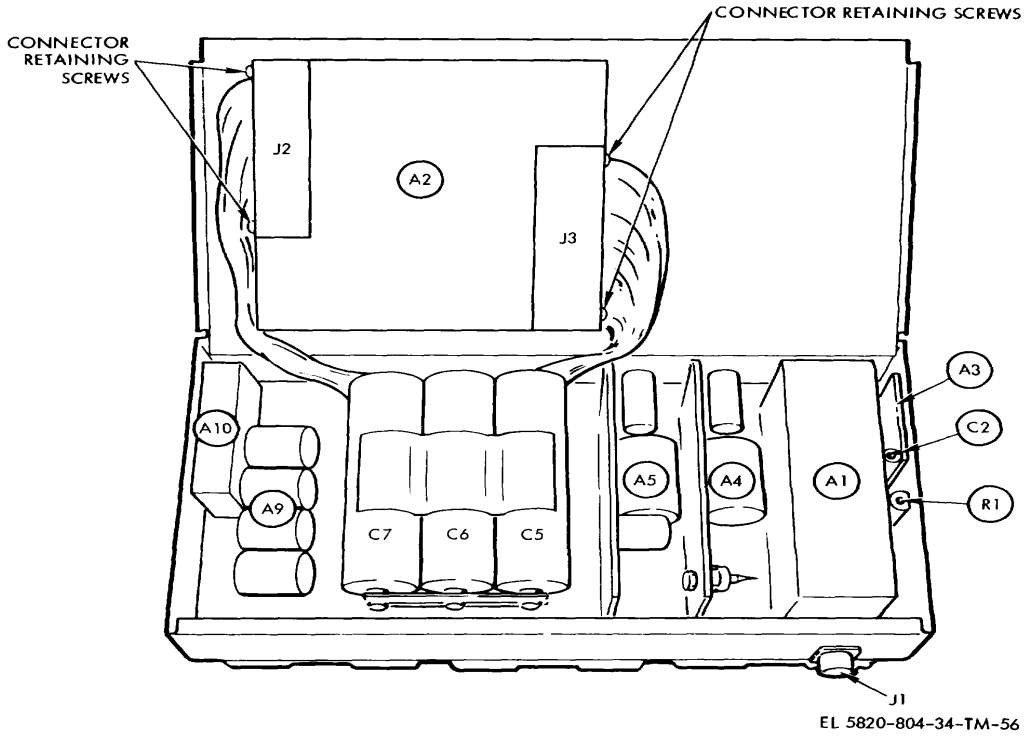

Figure 5-2. Power supply, top view with top cover open.

a. Transformer assembly, Al.
b. Printed circuit board, A2 (voltage regulator).
c. Circuit card assembly, A3 (starter circuit).
d. Component board assembly number 1, A4.
e. Component board assembly number 2, A5.
f. Heat sink assembly number 1, A6.
g. Heat sink assembly number 2, A7.
h. Heat sink assembly number 3, A8.
i. Terminal board assembly, A9 (filter capacitors).
j. SCR assembly, A10 (SCR overvoltage crow-bars).

5-3. Electrical Characteristics

The power supply converts input line power to the regulated dc operating levels required by the ICF modem. The dc output levels are + 5, -5, + 15, and -15 volts dc. The power supply is forced-air cooled and features overload and short-circuit protection circuitry. Refer to table 5-1 for a tabulation of performance characteristics.

Table 5-1. Performance Characteristics

Parameter	Characteristic
Ac input	120 volts ae +10%, 45 to 420 Hz, single phase.
De outputs	+15 volts de at 7 amps.
	-15 volts de at 5 amps.
	+5 volts de at 21 amps.
	-5 volts de at 5 amps.
Output regulation:	
Line and load	Less than ±0.1% for line input variation from 108 to 132 volts ac and loads of 10% to 90%.
Ripple and noise	10 mV rms.; 1.0 volt peak-to-peak.
Overvoltage trip:	
+5 and -5 volts de outputs	6 to 7 volts de.
+15 and -15 volts de outputs	17 to 18 volts de.
Current limit:	
+5 volts de output	24 to 26 amps.
-5 volts de output	5.8 to 6.3 amps.
+15 volts de output	8.0 to 8.8 amps.
-15 volts de output	5.8 to 6.3 amps

5-4. General

This section describes the operation of power sup-ply circuits. A functional block diagram description is followed by a detailed discussion of each functional circuit in the power supply.

5-5. Block Diagram Description

a. The power supply functionally consists of an input transient suppressor, a bridge rectifier and capacitor filter, two dc-to-dc converters, and four output voltage regulators (fig. 5-3). The ac input to the power supply is routed through a transient suppressor, which absorbs short-duration transients on the input line. The output of the transient suppressor is then rectified and filtered to produce a voltage level containing ripple at twice the frequency of the input source. This voltage level is fed to two dc-to-dc converters where it is chopped to produce a square wave that is subsequently rectified and filtered to generate true dc levels. Each dc-to-dc converter drives two series regulators that provide the plus and minus dc outputs required by the modem. The voltage regulators maintain constant output levels regardless of fluctuations in source voltage, output loading, and temperature.

b. Included in the power supply is a starter circuit that has no affect on power supply operation. This starter circuit is used in the initial checkout of the power supply by the manufacturer, and is by-passed by the addition of a jumper prior to final test and shipment.

WARNING

The bridge rectifier and capacitor filter perform full wave rectification of the ac input without using an input isolation transformer, and the dc output from the capacitor filter does not have one side tied to chassis ground. Therefore, large potentials do exist between the floating ground and chassis ground.

5-6. Circuit Description

a. *Transient Suppressor.* The transient suppresser (fig. FO-28), which includes two filters, absorbs short duration transients that might otherwise damage circuits in the power supply. Back-to-back Zener diodes (CR1) absorb the energy of high-amplitude low-frequency transients, so that they are not passed on to power supply input circuits. The filters, consisting collectively of L1, L2, C1, C2, C3, and C4, serve primarily to prevent high frequency switching transients, generated within the power supply, from being reflected back into the in-put line and into other equipment. The filters also prevent electromagnetic energy on the input line from being fed into the load circuits through the power supply.

b. *Bridge Rectifier and Capacitor Filter.* Diodes CR2, CR3, CR4, and CR5 form a full-wave bridge rectifier for the ac input (fig. FO-28). Capacitors C5, C6, and C7 provide filtering to remove or smooth out the remaining ac component in the output of the bridge rectifier. The filtered output is applied directly to the dc-to-dc converters through a jumper that bypasses the starter circuit (oscillator), which is used only for factory testing of the power supply.

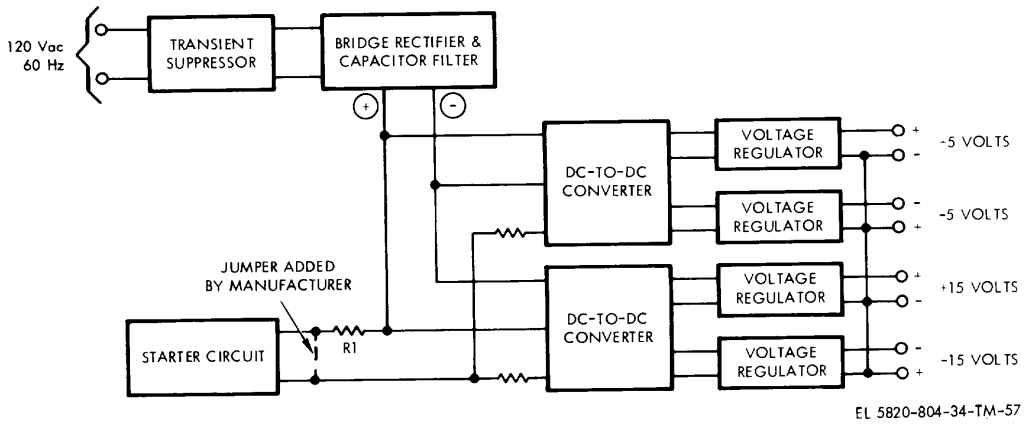

Figure 5-3. Dc power supply block diagram.

c . Dc-to-Dc Converter

(1) *General.* The dc-to-dc converters (fig. 54) transform the dc voltage derived from the input line power to specific dc levels required by the individual voltage regulators. The two-dc-to-dc converters accept the output of the bridge rectifier and capacitor filter circuit, generate a square wave signal, and then rectify and filter this signal to produce a dc level that is fed to the output voltage regulator circuits. One dc-to-dc converter is associated with the 5 and + 5 volts dc power supply outputs, and the other is associated with the 15 and + 15 volts dc outputs. The operation of both dc-to-dc converters is identical; therefore, only one is described.

(2) *Inverter components.* A dc-to-dc converter functionally consists of an inverter, two full-wave rectifiers, and an output filter. The inverter is a push-pull switching inverter that provides two square wave outputs and is comprised of two power transistors (Q4 and Q5) and two transformers (T1A and TIB) containing a core material that has a rectangular hysteresis loop characteristic. Transistors Q4 and Q5 function as multivibrator type switches and are controlled by feedback current coupled to their bases from the composite action of the two saturating transformers.

(3) *Inverter switching.* Switching action starts in the inverter because of a small inherent imbalance in the circuit that causes one of the transistors, for example Q4, to start conducting before the other. The resulting voltage induced in the secondary winding (29 and 30) of transformer T1A is applied to the primary of base-drive transformer T1B that is in series with feedback resistor R164. The secondary windings of TIB are connected so that transistor Q5 is reverse-biased and held at cutoff, while Q4 is driven to saturation. As transformer T1B saturates, the rapidly increasing primary current causes a greater voltage drop across feedback resistor R164. This increased voltage drop across R164 reduces the voltage applied to the primary of T1B, thus reducing the base drive input in Q4, which in turn decreases the collector current as Q4 eventually reaches cutoff. The curtailing of the collector current of Q4 causes the field of TIA to collapse, thereby reversing the polarity across the windings of transformers T1A and T1B. Transistor Q4 is then held at cutoff, while Q5 is rapidly driven to saturation. The transistors operate in this condition until transformer TIB saturates, and the circuit then returns to the initial state and the cycle is repeated.

(4) *Start resistor.* Resistor R8 assures a positive start for both transistors in the inverter when input power is applied. Then the circuit imbalance and regenerative action previously described causes the inverter to begin the switching action.

(5) *Square wave conversion.* The square wave output of the inverter is rectified and filtered. The full-wave rectifier associated with the + 15 volts dc output consists of CR17 and CR18, and the one associated with the 15 volts dc output consists of CR19 and CR20. RC snubbers, such as C13 and C17, are connected in parallel with each diode to dampen the transients that occur when a rectifier goes from the recovery to the blocking state upon each transition of the inverter square wave. Output filtering is provided by L8 and C22, and L7 and C21.

d. *Output Voltage Regulator.*

(1) *General.* The voltage regulator (fig. FO29), provided for each of the four output voltages, also includes both short circuit and overvoltage protection circuitry. Figure 55 is a simplified block diagram of the functional circuit groups in the voltage regulator. All four voltage regulators incorporate the same functions and operate similarly, therefore the following circuit description applies to each.

(2) Regulator circuits.

(a) The voltage regulator for the + 15 volt de output is used as an example in this circuit description. This series type regulator is comprised of a monolithic circuit element (IC2); transistors Q20, Q21, Q10, Q13; and interconnecting discrete components (fig. 56). The integrated circuit element IC2 is a multifunction component that has equivalent circuitry as shown in figure 56, which is a simplified schematic representation of the regulator circuit. Circuit element IC2 includes a built-in reference voltage source, error amplifier, and series pass transistor. This device also provides for output current limiting by driving an internal currentlimiting transistor from an external current-sensing resistor. Resistors R55, R56, R64 and R84 contribute to setting the allowed upper current level that flows through current-sensing resistor R88. Resistor R88, in conjunction with R89, also splits the load current through transistors Q20 and Q21. Whenever the upper current level is exceeded, causing the currentlimiting transistor within IC2 to conduct, the output voltage from the regulator is reduced. If the voltage reduction to compensate for the over-current load is large enough, the short circuit (under-voltage) detector ((4) below) will shutdown the voltage regulator through Q13 to prevent excessive power buildup in the series pass control element. The currentlimiting feature of IC2 protects the output regulator from overload conditions within the range of a short circuit up to an over-current load which turns on the under-voltage detector.

(b) A temperature-compensated reference voltage is fed through R71 as one input to the error amplifier in IC2. The other input to the error amplifier is taken from the sampling resistor network consisting of R70, RI3, and R12, which collectively

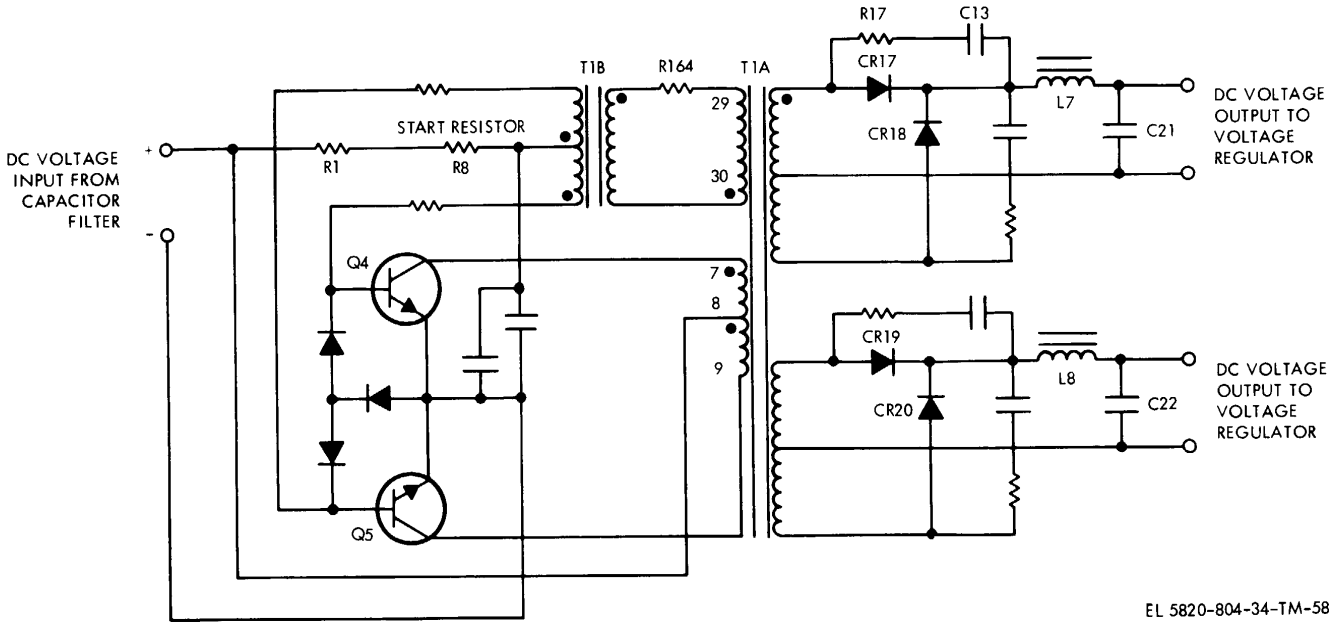

Figure 5 -4. Example of dc-to-dc converter.

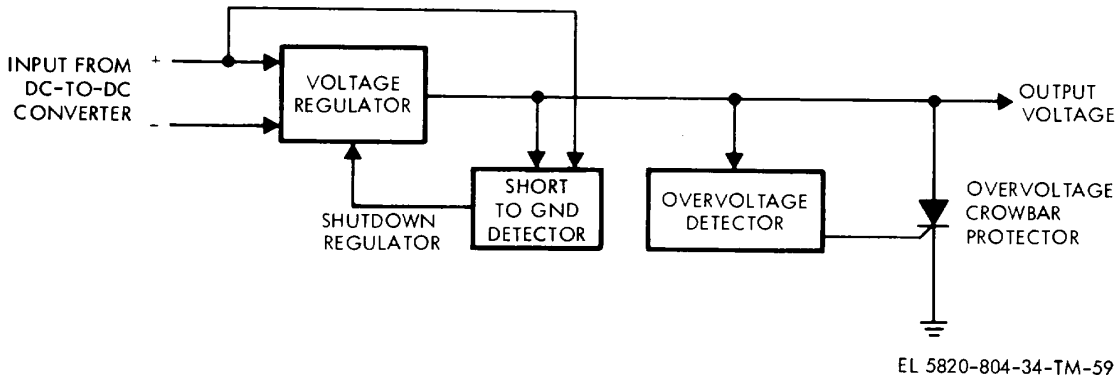

Figure 5-5. Regulator and output circuit block diagram.

sample a portion of the regulators output voltage. The error amplifier produces a signal that is proportional to the difference between the two inputs. The error amplifier output drives transistor Q10, which inverts the signal so that it is properly phased for negative feedback and amplifies it to drive the series pass control element (Q20 and Q21). The control element interprets the signal and compensates accordingly to maintain the output voltage at a near constant level for temperature, input line, and load current variations.

(c) The sampling resistor network of R70, R13, and R12 determine the closed-loop regulator gain. The output voltage can be varied by adjusting potentiometer R12. The RC network of R71 and C15 controls the rate of rise of the reference voltage generated within IC2, when power is first applied to the output regulator. This in turn controls the rate of rise of the regulator output voltage, and prevents the overvoltage detector circuit ((3) below) from detecting a false overvoltage condition at power turn-on.

(d) If the power supply output is shorted to ground, transistor Q13 is turned on by a signal from the under-voltage detector. When Q13 is turned on, the series pass control element (Q20 and Q21) is turned off, removing the load from the output regulator to prevent internal damage.

(e) Capacitor C14 presents a very low output impedance for sudden changes in load current, thus preventing large changes in output voltage when abrupt load changes occur. Capacitor C14, in conjunction with components R63, C11, R61 and C10, reduces the tendency of the regulator loop to oscillate during heavy loads. Resistor R63 also aids in limiting the current through Q13 and the base-to-collector junction of the current-limiting transistor in IC2, when Q13 is turned on and C14 discharges through them. Diode CR5 prevents C14 from charging in the reverse direction.

(3) *Overvoltage protector.*

(a) To prevent the modem circuits from being exposed to an overvoltage condition if a power supply output regulator fails, an overvoltage protection circuit is used. The overvoltage protection circuit for the + 15 volt dc power supply is shown in figure 5-7, and is typical of the same circuits used in the other three output regulators.

(b) Transistors Q1, Q2 and Q3 form a voltage comparator. The trip-level voltage of the comparator is determined by resistors R5, R6, R2, and R3. The voltage applied to the base of Q3 is less than that applied to CR2 during normal operation, therefore Q1 is cutoff, Q2 conducts, and SCR CR51 does not conduct. When the voltage output from the regulator exceeds the preset overvoltage limit, the voltage at the base of Q3 becomes more positive than the reference voltage of diode CR2, thus transistor Q2 is cutoff and Q3 and Q1 conduct. The conduction of transistor Q1 drives the SCR (CR51) into conduction, which reduces the output voltage.

(4) *Under-voltage detector.* The simplified circuit shown in figure 5-8 is the under-voltage detector used for the + 15 volt voltage regulator, and is typical of the under-voltage detectors employed in the other dc-voltage sources. This circuit serves to protect the output regulator from damage if a short circuit develops across the external load. Capacitors C8 and C9 prevent the turn-off of the voltage regulator (through Q13) during initial power turn-on. After power turn-on, CR4 conducts and turns on transistor Q4. With Q4 conducting, Q12 is held cutoff. When either a short circuit develops across the load, or the current-limiting action of the voltage causes the regulator output voltage to fall below the voltage value of CR4, transistor Q4 cuts off causing Q12 to conduct. When Q12 conducts, a signal is applied to turn on transistor Q13 in the voltage regulator, which effectively shuts down the regulator to prevent damage.

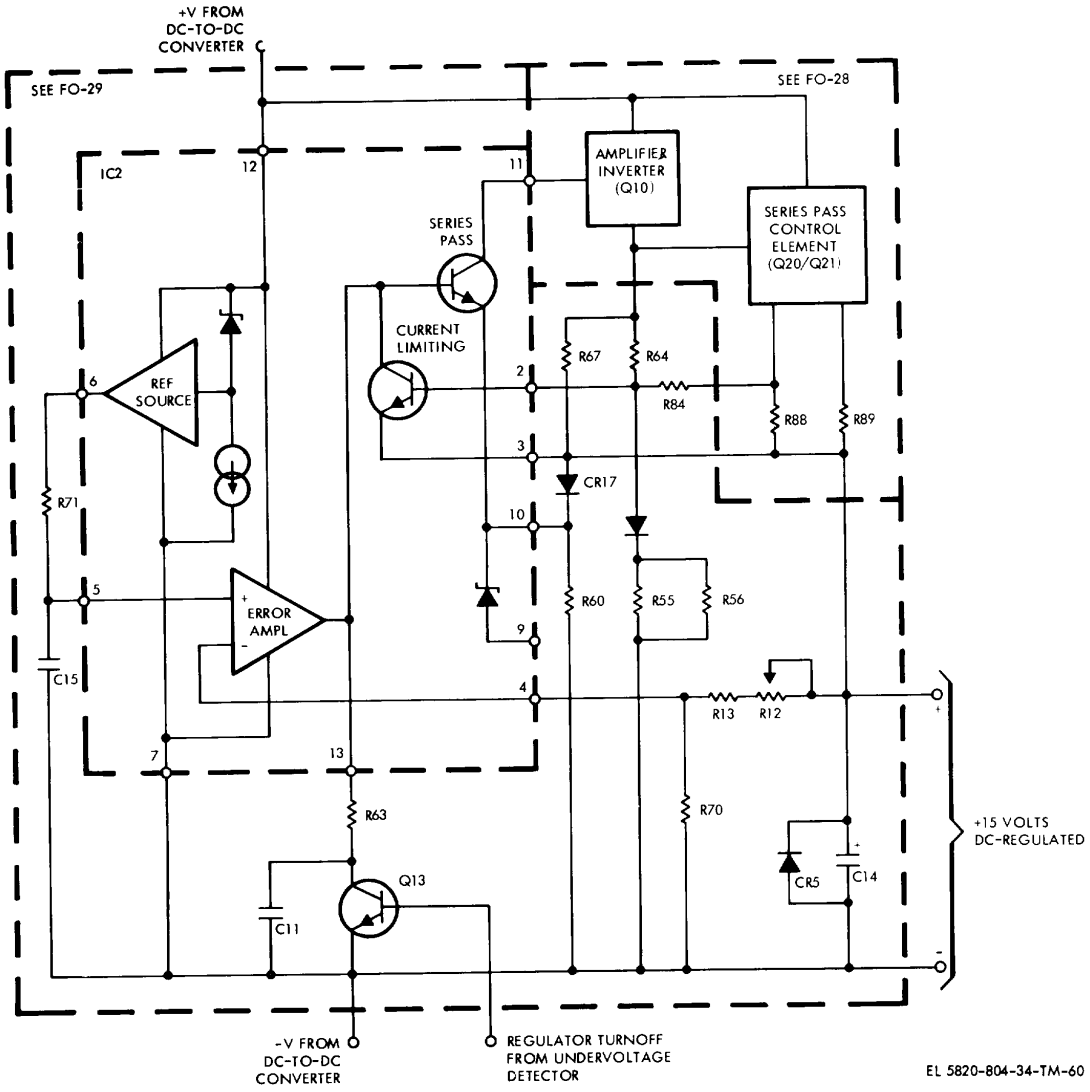

Figure 5-6. + 15 volt voltage regulator.

Section III. DIRECT SUPPORT MAINTENANCE INSTRUCTIONS

5-7. General This section contains detailed maintenance instructions for performing direct support level maintenance on the power supply. This maintenance category includes testing, troubleshooting, and replacement operations. Direct support maintenance on the power supply is initiated through the failure of organizational maintenance to obtain the required outputs by adjustment, or because of other system problems, such as blown fuses, which indicate faulty power supply operation. A power supply suspected of faulty operation should first be bench checked in accordance with the performance test procedure of paragraph 59. Adjustments performed by direct support maintenance are limited to those external adjustments controlling the dc output levels. Internal adjustments, such as setting the overvoltage trip points and over-current limits, are not to be attempted at this maintenance category.

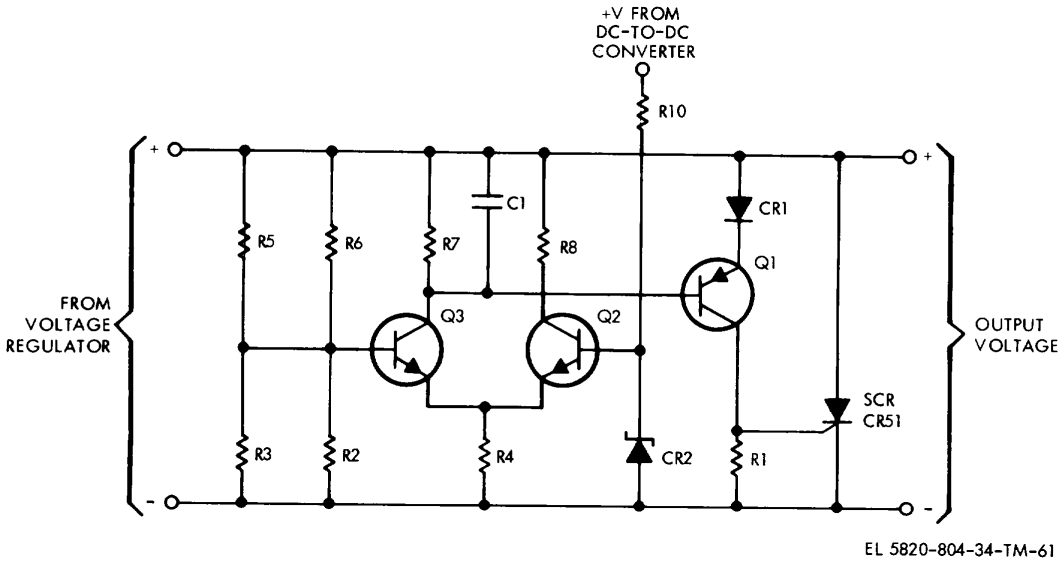

Figure 5-7. Overvoltage protector, simplified schematic diagram.

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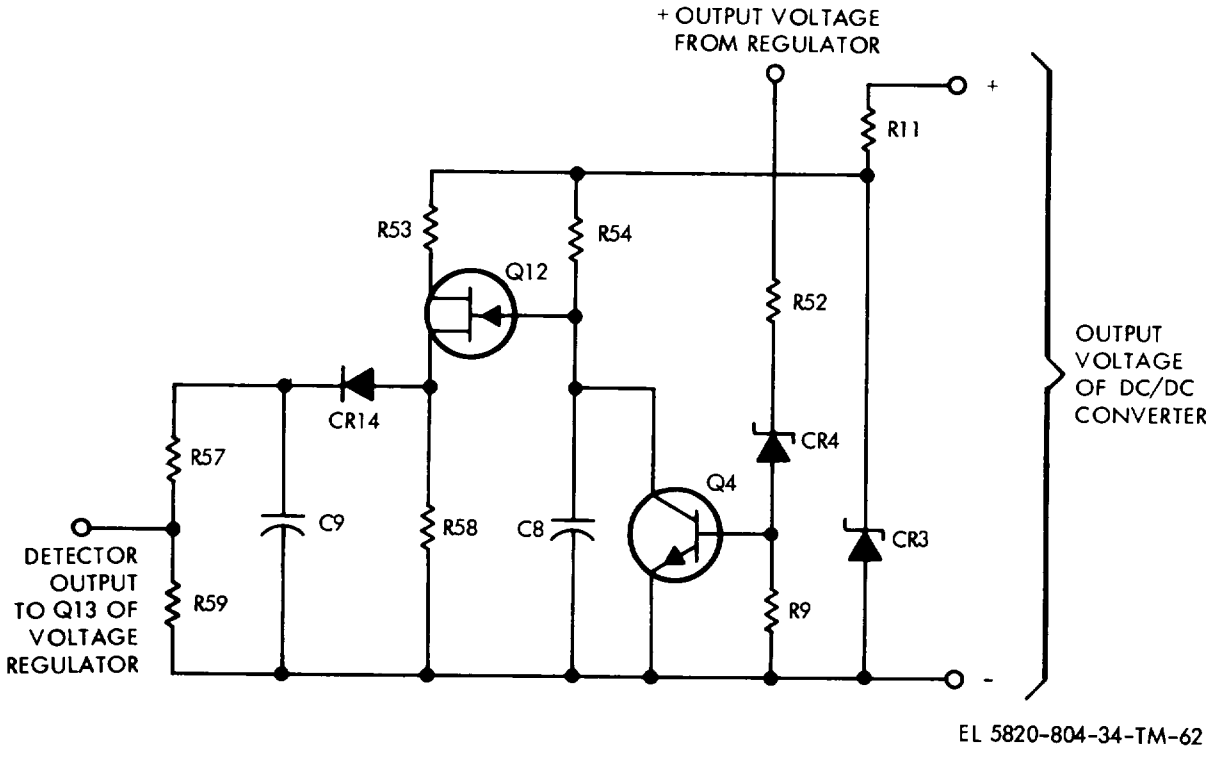

Figure 5-8. Example of undervoltage detector circuit..

5-8. Tools and Test Equipment

The equipment required for testing, troubleshooting, and repairing the power supply is listed below.

a. Oscilloscope, Tektronix 485A.
b. Multimeter, Simpson 270
c. Digital Voltmeter, Fluke 8000A-01.
d. Autotransformer, Variac W50M.
e. Power Supply/Oscillator Test Fixture, SM -D-882197.

5-9. Performance Testing

a. Pretest Information. The performance test procedure should be used in conjunction with the troubleshooting instructions to initially localize a fault. Also, each power supply shall be performance tested following any repair activity, to verify correct operation. Prior to testing a power supply, conduct a visual inspection for obvious defects and make repairs as required. First inspect the exterior of the assembly, and then remove the top cover (para 5-11 b) and inspect each subassembly. Look for blistered (overheated) components such as resistors and transistors, loose terminal connections, broken wires, and leakage of electrolyte from capacitors. Also ensure that heat sink fins are free of dust and dirt.

b. *Performance Test Procedure.*

WARNING

Primary and secondary voltage commons in this power supply are isolated from the chassis. Therefore, large potentials do exist between floating ground and chassis ground.

CAUTION

Whenever power is applied to a power supply, sufficient airflow must be provided to ensure adequate cooling. An external fan must be setup with airflow directed onto the power supply. Failure to observe this precaution will result in equipment damage.

(1) Verify that the AC POWER switch on the test fixture is in the off (down) position.

(2) Plug the test fixture line power cord into a 115 V ac source. Verify that the test fixture internal fan is operating.

(3) Connect equipment as shown in figure 5-9. Set the multimeter to the 50 V DC scale.

(4) Position an external fan so that the airflow passes directly over the power supply.

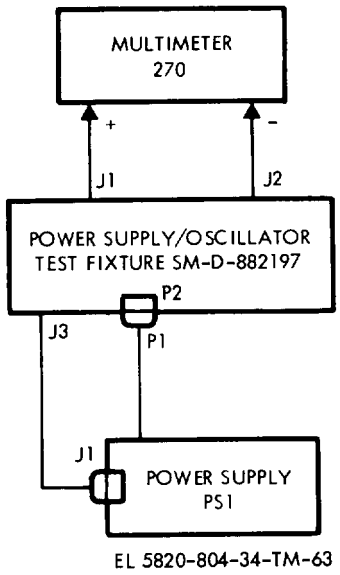

Figure 5-9. Initial test setup-power supply assembly test.

Output loading and adjustment test

(5) Set the test fixture AC POWER switch to the ON position, and set LOAD SELECT switch to position 14. Set the multimeter to the 10 V DC scale.

(6) Adjust the +5 V control on the power sup

ply for the lowest possible voltage, as indicated on the multimeter. Verify that the voltage is <4.9 volts dc.

(7) Adjust the +5 V control on the power supply for the highest possible voltage, as indicated on the multimeter. Verify that the voltage is >5.3 volts dc.

(8) Adjust the power supply +5 V control to obtain a reading of +5.1 +0.2 volts dc on the multimeter.

(9) Set test fixture LOAD SELECT switch to position 15. Verify that the multimeter indicates 5.1 +0.2 volts dc.

(10) Set test fixture LOAD SELECT switch to position 16. Verify that the multimeter indicates 5.1 +0.2 volts dc.

(11) Set test fixture LOAD SELECT switch to position 17, and verify a voltage reading of 5.1 +0.2 volts de.

(12) Set test fixture LOAD SELECT switch to position 10. The voltage to be measured is -5 volts dc, however, the polarity is reversed in the test fixture and therefore a positive voltage is indicated on the multimeter. Adjust the power supply -5 V control for +5.1 +0.2 volts dc as indicated on the multimeter.

(13) Adjust the power supply 5 V control for a minimum reading on the multimeter. Verify that the voltage is <4.9 volts dc.

(14) Adjust the power supply 5 V control for a maximum reading on the multimeter. Verify that the reading is >5.3 volts dc.

(15) Adjust the 5 V control of the power supply for a multimeter indication of 5.1 +0.2 volts dc.

(16) Set the multimeter to the 50 V DC scale, and set test fixture LOAD SELECT switch to position 6.

(17) Adjust the +15 V control on the power supply to obtain the lowest possible reading on the multimeter. Verify a minimum reading of +15.0 volts dc or less.

(18) Adjust the power supply +15 V control to obtain the maximum reading on the multimeter.
Verify a reading of +15.6 volts dc or more.

(19)Adjust the power supply +15 V control for a multimeter indication of +15.3 +0.1 volts dc.

(20) Set test fixture LOAD SELECT switch to position 7, and verify a reading of +15.3 +0.2 volts dc on the multimeter.

(21) Set test fixture LOAD SELECT switch to position 8, and verify a voltage indication on the multimeter of +15.3 +0.2 volts dc.

(22) Set test fixture LOAD SELECT switch to position 18, and verify a reading of +15.3 +0.2 volts dc on the multimeter.

(23) Set test fixture LOAD SELECT switch to position 19. Observe multimeter for a reading of 5.1 +0.2 volts dc.

(24) Set the multimeter to the 50 V DC scale, and set test fixture LOAD SELECT switch to position 20. The voltage being measured is 15 volts dc, however, the polarity is reversed in the test fixture so therefore the multimeter will indicate a positive voltage.

(25) Adjust the 15 V control of the power supply to obtain the lowest possible voltage indication. Verify that the lowest multimeter reading is <15.0 volts dc.

(26) Adjust the 15 V control of the power supply for the highest possible reading on the multimeter. Verify a reading >15.6 volts dc.

(27) Adjust the power supply 15 V control for a reading of 15.3 +0.2 volts dc.

(28) Refer to table 52, and set the test fixture LOAD SELECT switch to the specified positions and observe the multimeter for the associated voltage indications as a final check.

(29) Set the test fixture AC POWER switch to the off (down) position, and disconnect the test equipment.

Output ripple test

(30) Connect equipment as shown in figure 510.

(31) Adjust variac for 120 volts ac and set test fixture AC POWER switch to ON.

Table 5-2. Load Switching and Voltage Measurements

LOAD SELECT switch position	Voltage indication
10	15.3 +0.2 volts de
13	15.3 +-0.2 volts de
14	5.1 _+0.2 volts de
15	5.1 +0.2 volts de
16	5.1 +0.2 volts de
17	5.1 +0.2 volts de
18	15.3 +0.2 volts de
19	5.1 _+0.2 volts de
20	15.3 +0.2 volts de

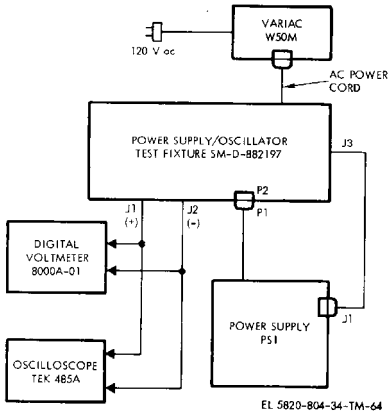

Figure 5-10. Test setup-output ripple regulation, and overvoltage trip point test.

(32) Refer to figure 511 for a typical example of an output waveform showing the ripple characteristics. Set the test fixture LOAD SELECT switch to each of the four positions listed in table 53 and use the oscilloscope to verify that any spikes on the selected output due to dc-to-dc converter switching are less than 1.0 volts peak-to-peak. Also, verify that any low level ripple due to input line frequency is less than 30 mV peak-to-peak on each selected output.

Table 5-3. Load Switching for Output Ripple Measurements

LOAD SELECT switch position	Dc output voltage
1	+5.1 +0.2 volts
4	+15.3 +0.2 volts
9	-5.1 +0.2 volts
11	-15.3 +0.2 volts

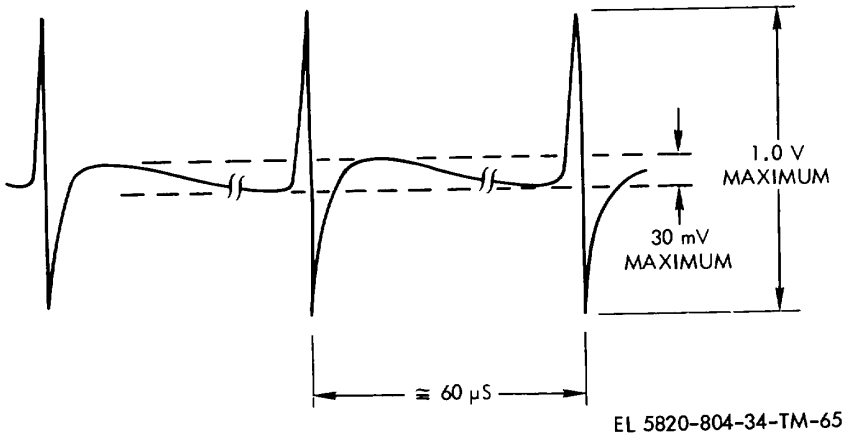

Figure 5-11. Typical dc output showing ripple characteristics.

Overvoltage trip point test

(33) Set LOAD SELECT switch on test fixture to position 1. While observing the output voltage on the digital voltmeter, slowly increase the + 5 V adjustment on the power supply until the output voltage begins to oscillate. Verify that the output was between 6.0 and 7.0 volts (overvoltage trip point) when the oscillation occurred. Readjust the + 5 V control for 5.1 +0.2 volts as read on the digital voltmeter.

(34) Repeat the procedure in (33) above for test fixture LOAD SELECT switch positions 4, 9, and 11, using the power supply +15 V, 5 V and 15 V adjustments, respectively. Verify that the trip point is between 17 and 18 volts for the +15 volt outputs (LOAD SELECT positions 4 and 11), and between 6.0 to 7.0 volts for the 5 volt output (LOAD SELECT position 9). After verifying the trip point for each output, readjust the appropriate voltage control on the power supply for the normal operating voltage, as listed below:

LOAD SELECT *switch position*	*Normal output voltage*
4	+15.3 ±0.2 volts
9	-5.1 +0.2 volts
11	-15.3±0.2volts

Regulation test

(35) Adjust the variac for 108 volts rms output.

(36) With the digital voltmeter, measure and record the power supply outputs at the +15 V, 15 V, +5 V, and 5 V test points on the power supply.

(37) Disconnect P1 from the test fixture.

(38) Adjust the variac for 132 volts rms output.

(39) With the digital voltmeter, measure and record the power supply outputs at the +15 V, 15 V, +5 V, and 15 V test points on the power supply

(40) Verify that the respective +5 volt and 5 volt measurements taken in (39) above are within +5 mV of the corresponding measurements taken in (36) above. Verify that the respective +15 volt and 15 volt measurements taken in (39) above are within +15 mV of the corresponding measurements taken in (36) above.

(41) Set test fixture AC POWER switch to the off (down) position, remove input to the variac, and disconnect all test equipment.

5-10. Troubleshooting

a. *General Trouble Analysis.* A faulty power supply shall first be bench checked in accordance with the performance test procedure in paragraph 59. Any out-of-tolerance parameters and abnormal operating conditions displayed during the performance test shall be noted. The fault isolation procedures in this paragraph are presented in tabular format and the individual table titles correspond to the most commonly encountered trouble symptoms observed during performance testing. Refer to figures FO28 and FO29 for schematic diagrams of the power supply. For parts location information and authorized repair parts lists, refer to TM 11582080434P. Appendix B, table B2 contains a wire list of internal power supply connections.

b. *Troubleshooting Procedures.*

(1) Detailed troubleshooting instructions are given in tables 54 through 517. These tables consist of step-by-step instructions for isolating faults to a subassembly or a component that is replaceable at the direct support. When a trouble symptom is identified, refer to the troubleshooting table title

that most closely corresponds to the symptom. In addition to the general and detailed troubleshooting tables, listings of typical point-to-point resistance and voltage measurements (tables 518 and 519) are provided as fault isolation aids. The troubleshooting tables are listed below.

(a) Table 54. Loss of +5 Volt Output, Troubleshooting Procedure.

(b) Table 55. Loss of 5 Volt Output, Troubleshooting Procedure.

(c) Table 56. Loss of +15 Volt Output, Troubleshooting Procedure.

(d) Table 57. Loss of 15 Volt Output, Troubleshooting Procedure.

(e) Table 58. Loss of + 5 and 5 Volt Complementary Outputs, Troubleshooting Procedure.

(f) Table 59. Loss of +15 and 15 Volt Complementary Outputs, Troubleshooting Procedure.

(g) Table 510. Loss of All Power Supply Outputs, Troubleshooting Procedure.

(h) Table 511. High Output Voltage, Troubleshooting Procedure.

(i) Table 512. All Output Voltages Low, Troubleshooting Procedure.

(i) Table 513. Low +15 and 15 Volt Complementary Outputs, Troubleshooting Procedure.

(k) Table 514. Low +5 and 5 Volt Complementary Outputs, Troubleshooting Procedure.

(1) Table 515. Low Output Voltage, Troubleshooting Procedure.

(m) Table 516. Output Voltage Oscillation, Troubleshooting Procedure.

(n) Table 517. Excessive Line Frequency Ripple On Outputs, Troubleshooting Procedure.

WARNING

High voltages are present within the power supply. Be extremely careful to avoid contact with high voltages when making internal measurements or adjustments with the top cover removed. Remove all power before performing any resistance or continuity checks, or any removal or replacement operations.

WARNING

Input filter capacitors PS1C5, C6, C7 of the power supply do not have one side () tied to chassis ground. Therefore large potentials do exist between this floating ground and chassis ground.

WARNING

Before disconnecting the electrical leads to input filter capacitors PS1C5, C6, or C7, allow at least 1 minute after removing power from the power supply for the capacitor voltage charge to bleed off.

Table 5-4. Loss of +5 Volt Output, Troubleshooting Procedures

Step	Symptom	Procedure	Probable cause/corrective action
1	Loss of +5 volt output	Measure voltage between J2-13 (-) and J2-14 (+) on voltage regulator board A2 Normal reading is 19 +2 volts dc.	If reading is normal or high, proceed to step 2 If reading is low, perform step 5.
2	Voltage between A2J2-14 and A2J2-13 is normal or high	Measure voltage between J2-13 (-) and J2-16 (+) on voltage regulator board A2. Normal reading is greater than 6 volts dc	If reading is normal, go to step 3 If reading is low, voltage regulator board A2 is defective or undervoltage detection circuit has been activated by an overcurrent condition. Replace voltage regulator board A2. If this does not correct fault, return original voltage regulator board to power supply and check components A1OCR49 and A9C51 for short circuits (see table 5-18 for typical output resistance measurements).
3	Voltage between A2J2-13 and A2J2-16 is normal	Measure voltage between J2-16 (+) and J2-17 (-) on voltage regulator board A2 Voltage is 0.8 +0.4 volt dc	If voltage reading is high, transistor A8Q12 is probable cause. If reading is normal, perform step 4.
4	Voltage between A2J2-16 and A2J2-17 is normal	Measure voltage between J2-17 (+) and J2-18 (-) on voltage regulator board A2 Normal voltage reading is 0.8 +0.4 volt dc	If voltage reading is normal, check for presence of 9.25 ±2.0 volts dc between A2J2-13 (-) and collector of transistor A8Q14. No voltage present indicates probable cause is broken wire between A1T1C-23 and collector of transistor A8Q14. If voltage reading is high, check for open connection between transistor A8Q12 emitter and A8Q14 base.
5	Voltage between A2J2-13 and A2J2-14 is low	Probable fault is shorted voltage regulator (A2 subassembly) input, or defective component in dc-to-dc converter circuits (faulty Al, A4, or A5 subassembly)	Replace subassembly A2 (voltage regulator). If fault is not corrected, return original subassembly A2 to power supply and return power supply to depot for repair.

Table 5-5. Loss of -5 Volt Output, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Loss of -5 volt output	Measure voltage between J3-13 (-) and J3-14 (+) on voltage regulator board A2. Normal voltage reading is 19.5 ±3 volts de.	If voltage reading is normal or high, perform step 2. If reading is low, perform step 5.
2	Voltage between A2J3-14 and A2J3-13 is normal or high	Measure voltage between J3-13 (-) and J3-16 (+) on voltage regulator board A2 mal reading is greater than 6 volts dc	If voltage reading is normal, perform step 3. If Nor-reading is low, voltage regulator board A2 is defective or undervoltage detection circuit has been tripped by an overcurrent condition. Replace a voltage regulator board A2. If this does not correct fault, return original voltage regulator A2 to power supply and check components A1OCR50 and A9C52 for short circuits (see table 5-18 for typical output resistance measurements).
3	Voltage between A2J3-13 and A2J3-16 is normal	Measure voltage between J3-16 (+) and J3-17 (-) on voltage regulator board A2 Normal reading is less than 12 volts dc.	If voltage reading is high, replace transistor A8Q13. If reading is normal, perform step 4.
4	Voltage between A2J3-16 and A2J3-17 is normal.	Measure voltage between J3-17 (+) and J3-18 (-) on voltage regulator board A2 Normal reading is less than 1.2 volts de	If voltage reading is high, transistor A7Q19 is probable cause. If reading is normal, resistor A7R87 is open and should be replaced. 5
	Voltage between A2J3-13 and A2J3-14 is low.	Probable fault is shorted voltage regulator (A2 subassembly) input or defective component in de-to-de converter circuits	Replace voltage regulator board A2. If fault is not corrected, return original subassembly A2 to power supply Power supply should be sent to depot for repair, as fault location procedure indicates trouble is defective Al, A4, or A5 subassembly.

Table 5-6. Loss of +15 Volt Output, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Loss of -15 volt output	Measure voltage between J2-4 (-) and J2-7 (+) on voltage regulator board A2. Voltage reading is 22.5 +3.0 volts de.	If voltage reading is normal or high, perform step 2. If reading is low, perform step 5.
2	Voltage between A2J2-4 and A2J2-7 is normal or	Measure the voltage between J2-6 (-) and J2-7 (+) of voltage regulator board A2 Normal reading is 0.8 +0.4 volt de	If reading is normal, perform step 3. If voltage is high or low, replace voltage regulator board high A2. If this does not eliminate fault, return original subassembly A2 to power supply, and check transistor A7Q10 for open or shorted base-to-emitter junction. If transistor A7Q10 appears good, check components A1OCR51 and A9C53 for short circuits (see table 5-18 for typical output resistance measurements).
3	Voltage between A2J2-6 and A2J2-7 is normal	Measure the voltage between J2-4 (-) and J2-5 (+) on voltage regulator board A2. Normal voltage reading is greater than 16 volts de.	If voltage is low, transistor A7Q10 is probable cause. If voltage is normal, perform step 4.
4	Voltage between A2J2-4 A2J2-5 is normal	Measure voltage between J2-5 (+) and J2-9 (-). Normal reading is 0.8 +0.4 volt dc	If voltage reading is normal, check resistors and A7R88, A7R89, and associated wiring for open circuit. If reading is high, check transistors A7Q20, A7Q21, and associated wiring for open circuit.
5	Voltage between A2J2-4 and A2J2-7 is low	Probable fault is shorted voltage regulator board A2 input or defective component in dc-to-dc converter circuits (faulty A1, A4, or A5 subassembly)	Replace voltage regulator board A2. If fault is not corrected, return original A2 subassembly to power supply, and return power supply to depot for repair.

Table 5-7. Loss of-15 Volt Output, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Loss of -15 volt output If	Measure voltage between J3-4 (-) and J3-7 (+) on voltage regulator board A2. Normal reading is 22.5 ±3.0 volts de.	If reading is normal or high, perform step 2 reading is low, perform step 5.
2	Voltage between A2J3-4 and A2J3-7 is normal or high	Measure voltage between J3-6 (-) and J3-7 (+) on voltage regulator card A2. Normal reading is 0.8 +0.4 volt dc	If reading is normal, perform step 3. If reading is high or low, replace voltage regulator A2 sub-assembly. If fault is not corrected, reinstall original A2 subassembly, and check transistor A7Q11 for shorted or open base-to-emitter junction. If A7Qll appears good, check components A10CR52 and A9C54 for short circuit (see table 5-18 for typical output resistance measurements).
3	Voltage between A2J3-6 A2J3-7 is normal.	Measure voltage between J3-4 (-) and J3-5 (+) on voltage regulator board A2. Normal reading is greater than 16 volts dc	If voltage reading is low, transistor A7Q11 is and probable cause If reading is normal, perform step 4.
4	Voltage between A2J34 A2J3-5 is normal.	Measure voltage between J3-5 (+) and J3-9 (-) of voltage regulator board A2. Normal reading is 0.8 +0.4 volt dc	If voltage reading is normal, check resistors an d A7R90 and A7R91 and associated wiring for open circuit. If reading is high, check transistors A7Q22 and A7Q23 and associated wiring for open circuit.
5	Voltage between A2J3-4 and A2J3-7 is low	Probable fault is shorted input to voltage regulator board A2 or defective compo-nent in dc-to-dc converter circuit (faulty A1, A4, or A5 subassembly)	Replace voltage regulator board A2. If fault is not corrected, return original A2 subassembly to power supply, and return power supply to depot for repair.

Table 5-8. Loss of +5 and -5 Volt Complementary Outputs, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Loss of both +5 and -5 volt outputs	Dc-to-dc converter not operating. Measure voltage between capacitors PSIC5, C6, C7 common I-) bus and transformer AIT1C-14. Normal voltage reading is 155 ±30 volts de.	If voltage reading is normal, perform step 2 If no voltage is present, check for broken wires or connections from PS1C5 (+) to A1TlC-14 and repair as required.
2	Voltage between capaci-tors PS1C5, C6, C7 common (-) bus and A1T1C-14 is normal. winding	Measure voltage between capacitors PS1C5, C6, C7 common (-) bus and transformer AlTlD-20. Normal reading is 0.6+0.3 volt dc	If voltage reading is normal, perform step 3. If reading is high check for; open resistor A6R10 or A6R12, open base-to-emitter junction on transistor A6Q6 or A6Q7, open transformer between A1T1D-19, AlT1D-20,or A1TlD-21 If voltage reading is not present, resistor A3R1 is open If transformer AIT1D winding or resistor A3R1 is open, return the power supply to the depot for repair.
3	Voltage between capaci-tors PSIC5, C6, C7 I-) bus and A1T1D-20 is normal	Remove input power from power supply and measure continuity between transformer windings as follows: A1TlD-17 to AlTlC-16. 1 ohm max A1T1C-14 to AlT1C-13 1 ohm max. A1T1C-14 to AlTlC-15 1 ohm max.	If any measurement exceeds 1 ohm, subassembly Al is faulty and power supply should be common returned to depot. If measurements are normal, perform step 4.
4	Transformer winding con-tinuity is normal	Check for the following possible faults: a. Shorted diode A6CR53 or A6CR55, or open A6CR54. b. Shorted base-to-emitter junction on transistor A6Q6 or A6Q7. c. Open base-to-collector junction on tran-sistor A6Q6 or A6Q7. d. If items above are normal, check for open resistor A1R165.	a Replace faulty diode. b Replace faulty transistor. c Replace faulty transistor. d Return power supply to depot for repair.

Table 5-9. Loss of +15 and - 15 Volt Complementary Outputs, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Loss of both +15 and -15 volt outputs	Dc-to-dc converter not operating or +15 volt output has failed. Measure voltage between J3-4 (-) and J3-7 (+) on voltage regulator board A2. Normal reading is greater than 18 volts.	If reading is normal, refer to table 5-6. step 1If reading is low or zero, perform step 2 below.
2	Voltage between A2J3-4 and A2J3-7 is low or zero.	Dc-to-dc converter not operating. Measure voltage between capacitors PSIC5, C6, C7 common (-) bus and transformer A1T1A-8. Normal reading is 155 +30 volts dc	If voltage reading is normal perform step 3 If no voltage is present, check for broken wires or connections between capacitor PSIC5 (+) and transformer A1T1A-8.
3	Voltage between capacisistor PSlC5, C6, C7, (-).C6, bus and transformer A1T1A -8 is normal.	Measure voltage between capacitors PSIC5, C7 (-) bus and transformer A1T1B-26. Normal reading is 0.6 +0.3 volt dc	If voltage reading is normal, perform step 4. If reading is high, check for open resistor A6R9or A6R11, open base-to-emitter junction on transistor A6Q4 or A6Q5, open transformer winding between A1T1B-26, A1T1B-25, or A1T1B- 27. If no voltage is present, open resistor A3R8 is probable cause If transformer A1T1B winding or resistor A3R8 is open, return the power supply to the depot for repair.
4	Voltage between capacitors PSIC5, C6, C7 common (-) bus and A1T1B-26 is normal	Remove input power from power supply and measure continuity between transformer windings as follows: A1T1B-28 to A1T1A-29 1 ohm max A1T1A-8 to A1T1A-7 1 ohm max. A1T1A-8 to A1TlA-9 1 ohm max.	If any measurement exceeds 1ohm,subassembly A1 is defective and power supply should be returned to the depot for repair. If all measurements are normal, perform step 5.
5	Transformer winding continuity is normal	Check for the following possible faults: a. Shorted diode A6CR56 or A6CR58 or open diode A6CR57. b. Shorted base-to-emitter junction on transistor A6Q4 or A6Q5. c. Open base-to-collector junction on transistor A6Q4 or A6Q5. d. If items above are normal, check for open resistor A1R164.	a. Replace defective diode. b. Replace defective transistor. c. Replace defective transistor. d. Return power supply to depot for repair.

Table 5-10. Loss of All Power Supply Outputs, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	No de outputs	Check for open ac line power fuse	Replace ae line fuse. If fuse blows. upon application of power, perform step 2. If ac line fuse is not open, perform step 7.
2	Ac line fuse blows on power application	Remove input power from power supply and disconnect two pairs of leads from the (+) bus of capacitors PSIC5, C6, and C7. Reapply input power to power supply	If ac line fuse blows, short circuit is in transient suppressor or bridge rectifier circuits; return power supply to depot for repair. If ac line fuse does not blow, fault is in capacitors PSIC5, C6, C7; dc-to-dc converter circuits; or voltage regulator input. Perform step 3.
3	Input line fuse does not blow with capacitor PS1C5, C6, C7 + bus disconnected.	Check capacitors PSiC5, C6, and C7 for high leakage or shorts. Leakage resistance is less than 100K ohms	If capacitor PSiC5, C6, or C7 shows evidence of leakage or shorting, replace faulty components. If capacitors are good, perform step 4.
4	Capacitors PS1C5, C6, and C7 not faulty	Check between following points for indicated resistance: A2J2-13 to A2J2-14 2000 ohms min A2J3-13 to A2J3-14 2000 ohms min A2J2-4 to A2J2-7 2000 ohms min. A2J3-4 to A3J3-7 2000 ohms min.	If all resistance measurements are satisfactory, perform step 6 If a measurement is less than the indicated value, note the particular measurement and perform step 5.
5	Resistance measurement in step 4 not satisfactory	Remove voltage regulator board A2 and. repeat abnormal measurement taken in step 4 on the power supply	If measurement is now satisfactory, fault is in voltage regulator board A2. Replace faulty voltage regulator board A2. If the measurement is still low, the fault is in subassembly A4 or A5. In this case, return the power supply to the depot for repair.

Table 5-10. Loss of All Power Supply Outputs, Troubleshooting Procedure- Continued

Step	Symptom	Procedure	Probable cause/corrective action
6	Voltage regulator board A2 resistance measurements normal	Fault is in de-to-de converter switching circuits or transformers. Check the following for defects: a. Check transistors A6Q4, A6Q5, A6Q6, and A6Q7 for shorted junctions. b. Check diodes A6CR53 through A6CR58 for shorted junctions. c. Check transformers A1T1A through A1T1D for shorts	 a. Replace defective transistor. b. Replace defective diodes. c. Return power supply to depot if a transformer is shorted.
7	No dc outputs, input line fuse normal	Fault is open circuit in input bridge rectifier, transient suppresser, or chassis-mounted resistor PS1R1 Measure voltage across capacitors PSlC5, C6 and C7. Normal voltage is 155 ±20 volts de.	If voltage is normal or high, check for open chassis-mounted resistor PS1R1 or broken wires to transformers. If voltage reading is low, perform step 8.
8	Voltage across capacitors PS1C5, C6, and C7 is low	Check forward and reverse resistance (in-circuit) of rectifier diodes A4CR2, A4CR3, A4CR4, A4CR5. Normal forward resistance is 15 ohms maximum (RX1 scale); reverse resistance is 5K ohm minimum (RX100 scale).	If any resistance measurement is abnormal, probable cause is diode; return power supply to depot for repair. If resistance measurements are normal, perform step 9.
9	Bridge rectifier diodes forward and reverse resistance normal	Check continuity from ac input connector J1-1 to circuit junction of diodes A4CR3 and A4CR4, and from J1-2 to circuit junction of diodes A4CR2 and A5CR5	Open circuit indicates broken wire or open transient suppressor choke (A1L1 or A1L2) in subassembly A1..Repair broken wire as necessary. If transient suppressor choke is open, return power supply to depot for repair.

Table 5-11. High Output Voltage, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
		NOTE If output voltage exceeds overvoltage trip point, output will oscillate.	
1	Output voltage is high and cannot be reduced by output adjustment	Fault is in voltage regulator board A2 or caused by leaky output transistors Replace voltage regulator card A2	If output voltage can be adjusted to within required limits by output voltage adjustment, original voltage regulator board A2 is defective. If new voltage regulator board A2 does not correct fault, return original regulator board to power supply and perform step 2.
2	Voltage regulator board A2 not defective	To detect any shorted or leaky output transistors, make the following voltage checks at the specified points on the voltage regulator board A2 connectors. A voltage reading less than the designated value or one with reversed polarity indicates a shorted or leaky output transistor(s).	
		Output circuit / Measurement points / Voltage reading	
		+5 volt / J2-18 (-) to J2-17 (+) / -0.4	Perform step 3.
		J2-17 (-) to J2-16 (+) / +0.4	Replace transistor A8Q12.
		-5 volt / J3-18 (-) to J3-17 (+) / +0.4	Replace transistor A7Q19.
		J3-17 (-) to J3-16 (+) / +0.4	Replace transistor A8Q13.
		Output circuit / Measurement points / Voltage reading	
		+15 volt / J2-9 (-) to J2-5 (+) / -0.4	Perform step 3.
		J2-6 (-) to J2-7 (+) / +0.4	Replace transistor A7Q10.
		-15 volt / J3-9 (-) to J3-5 (+) / +0.4	Perform step 3.
		J3-6 (-) to J3-7 (+) / +0.4	Replace transistor A7Qll.
3	Voltage checks in step 2 indicate faulty output transistors	To isolate a particular faulty transistor in output stages consisting of multiple parallel-connected transistors, such as the +5, +15, and -15 volt supplies, monitor the	If the collector for a faulty transistor is disconnected, the associated high output voltage will decrease When this occurs, replace the applicable transistor.

Table 5-11. High Output Voltage, Troubleshooting Procedure- Continued

Step	Symptom	Procedure	Probable cause/corrective action
		output voltage of the supply and disconnect the collector leads of the parallel transistors one at a time. After each collector lead is disconnected, check for a decrease in the abnormally high output. When performing this check, only one collector should be disconnected at any one time. The three groups of parallel-connected output transistors are listed below. +5 volt supply: A8Q14, Q15, Q16, Q17, Q18. +15 volt supply: A7Q20, Q21. -15 volt supply: A7Q22, Q23.	

Table 5-12. All Output Voltages Low, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Low output, all voltages	Fault is low line voltage, bridge rectifier diode open, or open filter capacitor. Verify input voltage.	If input line voltage is normal, go to step 2.
2	Input line voltage normal	Check capacitors PS1C5, C6, and C7 for open condition. (See A, figure 5-13 for typical oscilloscope wave-form and table 5-18 for resistance measurement to aid in checking capacitors.)	Replace faulty capacitor. If no capacitor is faulty, return power supply to depot for bridge rectifier diode fault isolation and repair.

Table 5-13. Low +15 and -15 Volt Complementary Outputs, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Low +15 and -15 volt outputs	Probable fault is in dc-to-dc converter oscilloscope verify presence of 310 volt peak-to-peak square wave (see A, figure 5-12) at A1T1A-9 and A1T1A-7, using (-) bus of PS1CS, C6, C7 as ground reference At both measurement points the low part of wave-form should be less than 3 volts, indicating transistors A6Q5 and A6Q4 are saturating.	With If wave-form indicates absence of transistor saturation at both A1T1A-9 and A1T1A-7, check diode A6CR57 for open or shorted condition and check resistors A6R9 and A6R11for correct values. If correct wave-form is not present at only one point (A1T1A-7 or AlT1A-9), proceed to step 2 or 3 as applicable.
2	Wave-form at A1T1A-9 does not indicate transistor saturation	Transistor A6Q5 not saturating. Check for open diodes A6CR57, A6CR56, A6CR58. Also check for leaky transistor A6Q4 or low gain of transistor A6Q5. {See B and C, figure 5-12 for typical waveshapes in troubleshooting components.)	Replace defective component(s) as necessary.
3	Wave-form at A1T1A-7 does not indicate transistor saturation	Transistor A6Q4 not saturating. Check for open diodes A6CR56, A6CR57, A6CR58. Also check for leaky transistor A6Q5 or low gain of transistor A6Q4. (See B and C, figure 5-12 for typical waveshapes in troubleshooting components.)	Replace defective components as necessary.

Table 5-14. Low +5 and -5 Volt Complementary Outputs, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Low +5 and -5 volt outputs	Probable fault is in dc-to-dc converter. With oscilloscope verify presence of 310 volt peak-to-peak square wave (see A, figure 5-12} at A1T1C-13 and A1TlC-15, using (-) bus of PSIC5, C6, C7 as ground reference. At both measurement points the low part of waveform should be less than 3 volts, indicating transistors A6Q6 and A6Q7 are saturating.	If waveform indicates absence of transistor saturation at both AlTIC-15 and A1TlC-13, check diode A6CR54 for open or short condition and check resistors A6R10 and A6R12 for correct values. If normal waveform is not present at only one point (AITIC-15 or AlT1C-13), proceed to step 2 or 3 as applicable.
2	Waveform at A1T1C-13 does not indicate transistor saturation	Transistor A6Q6 not saturating. Check for open diodes A6CR53, A6CR54, A6CR55. Also check for leaky transistor A6Q7 or low gain of transistor A6Q6. (See B and C, figure 5-12 for typical waveshapes in troubleshooting components.)	Replace defective components as necessary.
3	Waveshape at A1T1C-15 does not indicate transistor saturation	Transistor A6Q7 not saturating. Check for open diodes A6CR53, A6CR54, A6CR55. Also check for leaky transistor A6Q6 or low gain of transistor A6Q7. (See B and C, figure 5-12 for typical waveshapes in troubleshooting components.)	Replace defective components as necessary.

Table 5-15. Low Output Voltage -Single Output, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Low output voltage on single output	Fault is in voltage regulator board A2, rectifier circuit in dc-to-dc converter, or output drive transistors. Replace voltage regulator board A2	If output voltage returns to normal, original voltage regulator is faulty If fault is not corrected, return original voltage regulator to power supply and perform step 2.
2	Voltage regulator board A2 is not defective	Make the following applicable voltage checks at the specified points on the voltage regulator board A2 connectors Output circuit — Measurement points — Voltage reading +5 volt — J2-13(-)toJ2-14(+) — 19 +3 -5 volt — J3-13 (-)toJ3-14(+) — 14.5 -2.5 +15 volt — J2-4 (-) toJ2-7(+) — 22.5 +3 -15 volt — J3-4 (-)toJ3-7(+) — 22.5 +3	If the measured voltage is low, fault is in subassembly A1, A4, or A5. Return the power supply to depot for repair. If the measured voltage is normal or high, perform step 3.
3	Voltage measured at voltage regulator input point is normal or high	Measure the following applicable voltage at the voltage regulator board A2 connectors, as indicated below Output circuit — Measurement points — Voltage reading +5 volt — J2-13 (-) to J2-17 (+) — 6.4 ±0.5 -5 volt — J3-13 (-) to J3-17 (+) — 6.4 ±0.5 +15 volt — J2-4 (-) to J2-5 (+) — 16.9 ±0.5 -15 volt — J3-4 (-) to J3-5 (+) — 16.5 ±0.5	If the voltage measured is low, the following applicable transistor is the probable cause: +5 volt output: transistor A8Q12. -5 volt output; transistor A8Q13. +15 volt output; transistor A7Q10. -15 volt output; transistor A7Qll. If the measured voltage is high, the following applicable transistors are probable causes: +5 volt output; transistors A8Q14 through A8Q18. -5 volt output; transistor A7Q19. +15 volt output; transistors A7Q20 and A7Q21. -15 volt output; transistors A7Q22 and A7Q23.

Table 5-16. Output Voltage Oscillation, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Output oscillates between approximately 0 volt And normal output level	Oscillation is result of output level adjustment set too high, high voltage fault, or faulty overvoltage detection circuit. Adjust output level adjustment on voltage regulator board A2 to reduce output to proper level.	If output adjustment does not affect oscillation problem, perform step 2.
2	Output adjustment does not affect oscillation	Observe output voltage on oscilloscope and determine if upper level of waveform exceeds overvoltage trip point (see table 5-1 for trip point limits)	If upper level exceeds overvoltage limit, refer to table 5-11. If upper level of waveform is below the overvoltage trip point, replace voltage regulator board A2. If voltage regulator substitution does not correct fault, reinstall original voltage regulator and perform step 3.
3	Voltage regulator board A2 substitution does not correct fault	Replace appropriate SCR crowbar diode: +5 volt supply: A10CR49 -5 volt supply: A1OCR50 +15 volt supply: A10OCR51 -15 volt supply: A10CR52	If SCR crowbar replacement does not correct fault, perform step 4.
4	SCR crowbar diode is not faulty	Check appropriate current limit resistor for open condition: +5 volt supply: A8R82 -5 volt supply: A7R87 +15 volt supply: A7R88 -15 volt supply: A7R90	Replace open resistor.

Table 5-17. Excessive Line Frequency Ripple on Outputs, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Excessive ripple on all outputs	Refer to table 5-12 for troubleshooting procedure (See figure 5-11 for allowable ripple limits on dc outputs.)	
2	Excessive ripple on single output.	Fault is defective voltage regulator board A2 or output filter. Replace voltage regulator board A2. (See figure 5-11 for allowable ripple limits on dc output.)	If excessive ripple is reduced, voltage regulator was faulty. If ripple is not reduced, reinstall original voltage regulator board. Probable cause is then the output filter capacitor (A9C51, A9C52, A9C53, or A9C54) associated with the de output containing the ripple.
3	Excessive ripple on complementary outputs	Probable cause is defective component in dc-to-dc converter. (See fig.5-11 for allowable ripple limits on de outputs.)	If ripple is present in +-15 volt complementary outputs, perform troubleshooting procedure in table 5-13. If ripple is present on +5 volt outputs, perform troubleshooting as outlined in table 5-14.

Table 5-18. Typical Resistance Measurements

From (+)	To (-)	Scale	Reading	Comments
PS1C5 (+)	PSIC5 (-)	R x 100	1200Q	
PS1JI-1	PSlJ1-2	R x 100	>100KQ	
PSlJ1-2	PSlJ-1	R x 100	>1OOKQ	
+5 V (TP)	COM (TP)	R x 100	950Q	
+15 V (TP)	COM (TP)	R x 100	1550Q	
-15 V (TP)	COM (TP)	R x 100	1650Q	
-5 V (TP)	COM (TP)	R x 100	950Q	
+5 V (TP)	COM (TP)	R x 10000	50 KQ	
+15 V (TP)	COM (TP)	R x 10000	150KQ	} With A2J2 and AZJ3 disconnected: allow 1 minute charge time.
-15 V (TP)	COM (TP)	R x 10000	150KQ	
-5 V (TP)	COM (TP)	R x 10000	50KQ	

Table 5-19. Typical Voltage Measurements

		Scale	Reading	
From (+)	To (-)	(+ dc)	(in volts)	Comments
PSIC5 (+)	PSIC5 (-)	250 V	155	120 V ac, 60 Hz input.
PSIR1 (top)	PS1C5 (-)	50 V	21	PS1RI located on right side of chassis.
A2J2-14	COM (TP)	50 V	19.0	+5 V regulator.
A2J2-16	COM (TP)	10 V	6.8	+5 V regulator.
A2J2-17	COM (TP)	10 V	6.3	+5 V regulator.
A2J2-18	COM (TP)	10 V	5.7	+5 V regulator.
A2J2-7	COM (TP)	50 V	22.5	+15 V regulator.
A2J2-6	COM (TP)	50 V	22.0	+15 V regulator.
A2J2-5	COM (TP)	50 V	16.9	+15 V regulator.
A2J2-9	COM (TP)	50 V	16.1	+15 V regulator.
A2J3-14	COM (TP)	50 V	14.5	-5 V regulator.
A2J3-16	COM (TP)	2.5V	1.75	-5 V regulator.
A2J3-17	COM (TP)	2.5V	1.25	-5 V regulator.
A2J3-18	COM (TP)	2.5V	0.6	-5 V regulator.
A2J3-7	COM (TP)	10 V	7.5	-15 V regulator.
A2J3-6	COM (TP)	10 V	6.9	-15 V regulator.
A2J3-5	COM (TP)	2.5V	1.15	-15 V regulator.
A2J3-9	COM (TP)	2.5V	0.60	-15 V regulator.

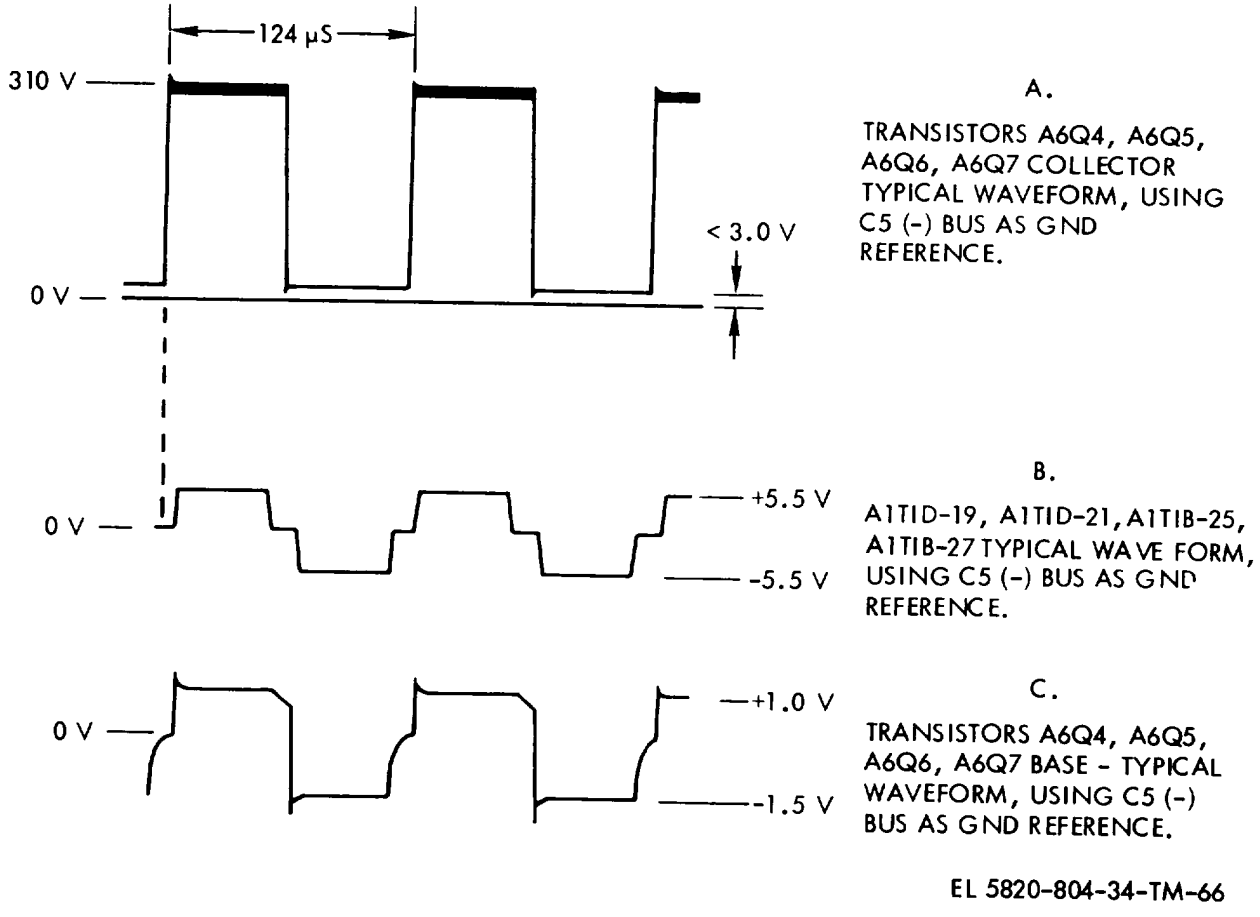

Figure 5-12. Dc-to-dc converter-typical waveforms.

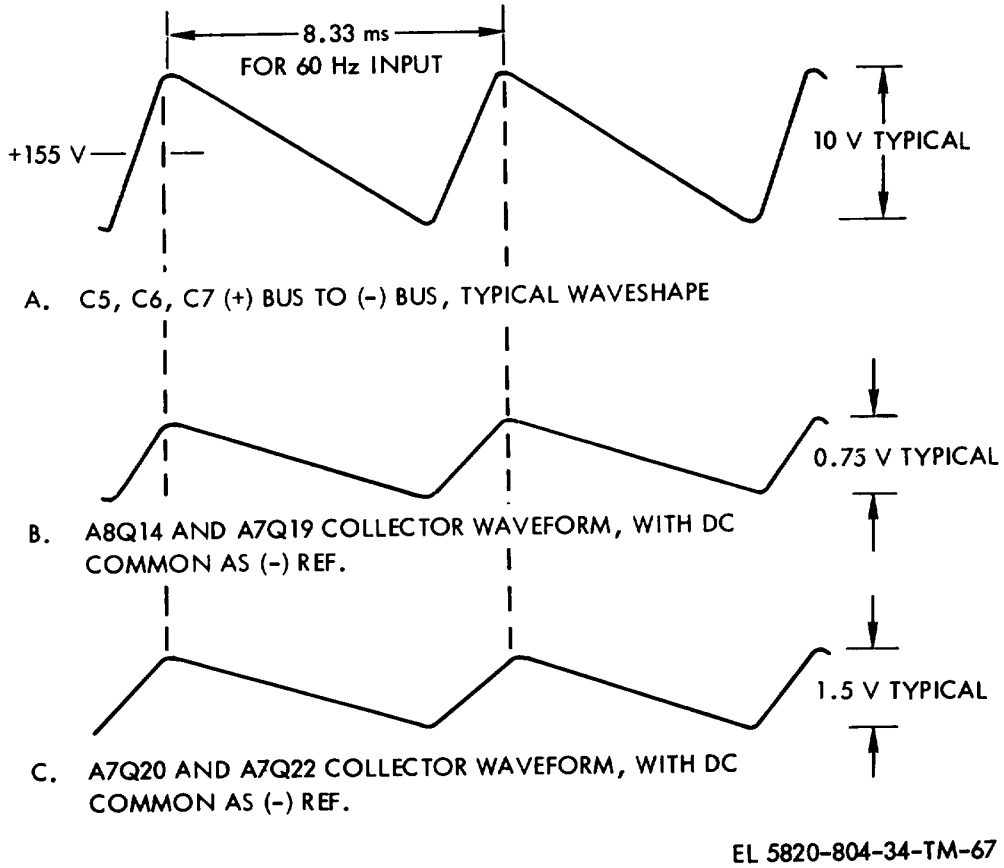

Figure 5-13. Typical input filter and output drive circuit waveforms.

(2) To perform certain measurements as required in the troubleshooting procedures, removal of the power supply top cover and partial removal of other subassemblies are necessary. Removal and replacement procedures are covered in paragraph 511. For all resistance and voltage measurements required in the troubleshooting procedures, use a multimeter unless otherwise specified. All component reference designators in the troubleshooting procedures are prefixed with the pertinent subassembly reference designator to aid in the physical location of components.

5-11. Removal and Replacement Procedures

a. *Power Supply* PS1. To remove or replace the power supply, refer to the instructions in paragraph 39b.

b. *Power Supply Top Cover*. Remove the 13 screws labeled A in figure 514. Lift top cover and swing back to position shown in figure 52, revealing voltage regulator board A2. To replace the top cover, reverse the above procedure.

c. *Printed Circuit Voltage Regulator) Board* A2. Remove top cover as instructed in b above. Remove the two retaining screws (fig. 52) from each connector (A2J2 and A2J3) on the voltage regulator board and disconnect the cable connectors. Remove the seven screws labeled B in figure 514, to free the board from the top cover. Reinstall the voltage regulator board in the reverse order of removal.

d. Heat Sink Assemblies A 6, A 7, and A8.

(1) Remove two retaining screws (fig. 515) from one side of the heat sink assembly, then loosen the two retaining screws on the other side of the assembly. Slide the heat sink assembly sideways to free it from the loosened screws, and fold it out and away from the power supply chassis as shown in figure 515 for access to heat sink assembly components.

(2) When replacing power transistors on a heat sink assembly, be sure to install insulating washers with thermal compound applied to both sides of washers.

(3) Replace heat sink assemblies by reversing the instructions in (1) above.

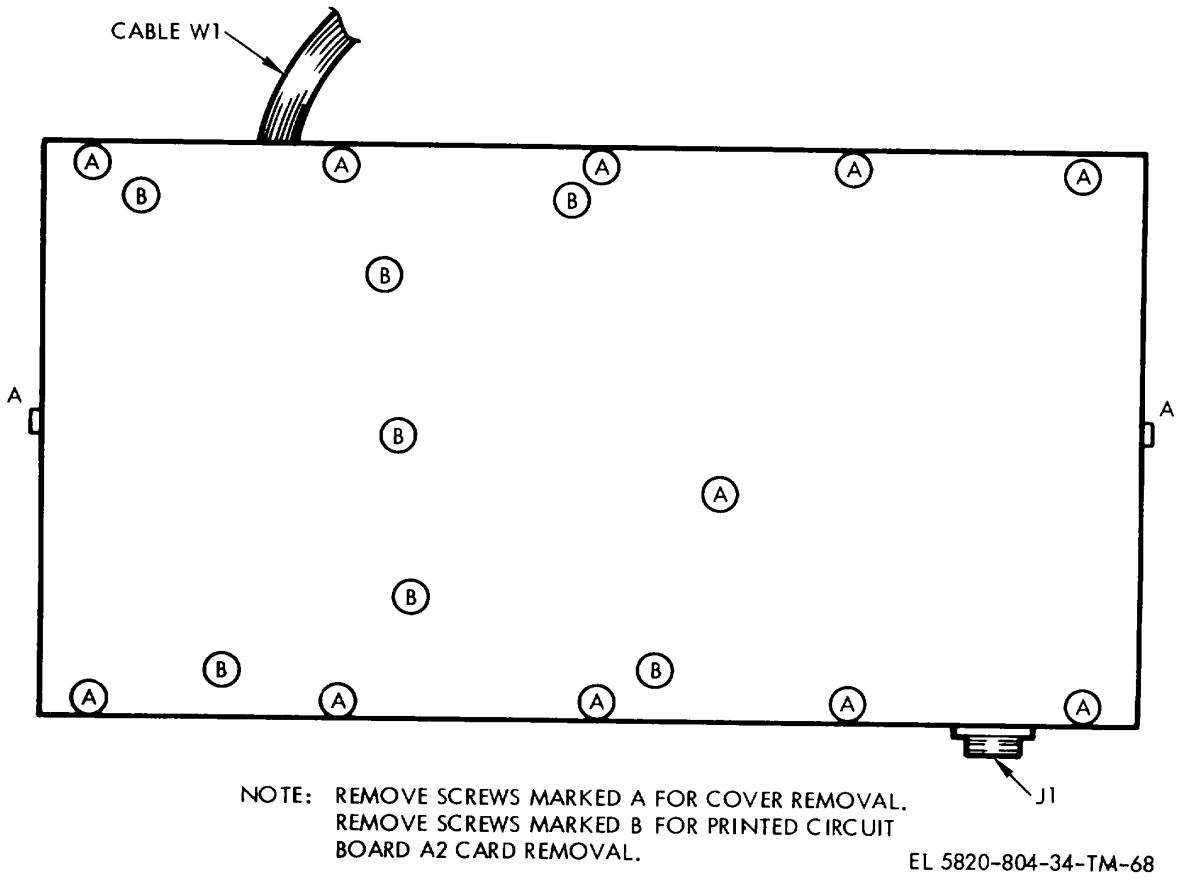

Figure 5-14. Top view power supply.

e. *Terminal Board Assembly A9.* Loosen and remove heat sink assembly A8 as described in d above, to expose terminal board A9 mounting screws. Remove the four mounting screws and nuts securing the terminal board to the chassis.

NOTE

It is generally possible to remove most of the components on the terminal board without removing the terminal board from the chassis.

f. SCR Mounting Assembly A10. Remove the two mounting screws located on the side of the power supply adjacent to the SCR mounting assembly. When replacing an SCR on the mounting assembly, be sure to install insulating washers with thermal compound applied to both sides of the washer. When replacing SCR CR49, bend the long lead on CR49 to prevent interference with the top cover of the power supply. While bending the lead, support the lead between the glass seal and the bend to prevent cracking the seal.

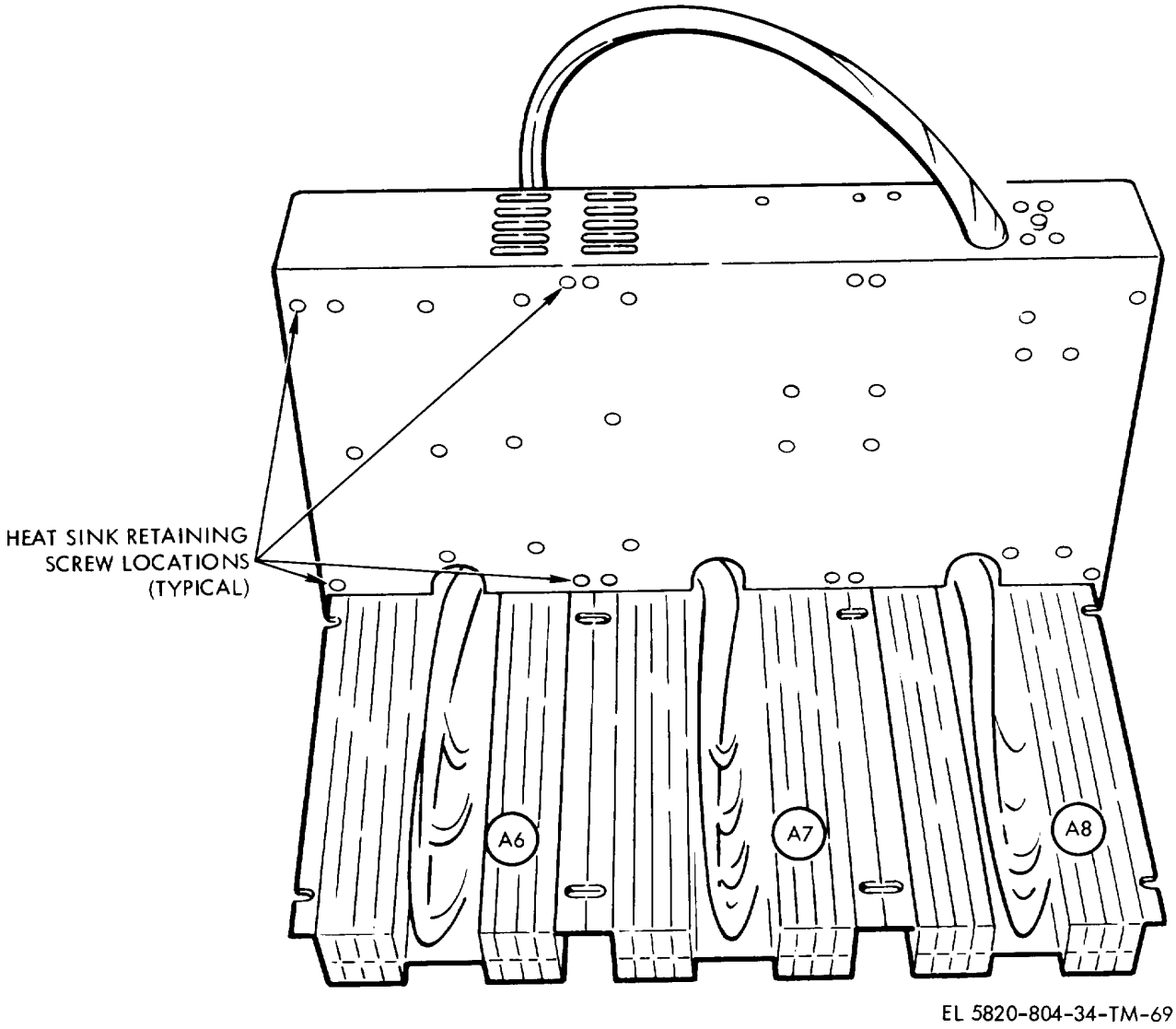

Figure 5-15. Bottom of power supply chassis with heat sinks folded out.

APPENDIX A

REFERENCES

DA Pam 310-4	Index of Technical Manuals, Technical Bulletins, Supply Manuals (Types 7, 8, and 9), Supply Bulletins, and Modification Work Orders.
DA Pam 310-7	US Army Index of Modification Work Orders.
TM 11-5820-803-12	Operator and Organizational Maintenance Manual for Modem, Digital Data MD-921/G.
TM11-5820-804-12	Operator and Organizational Maintenance Manual for Modem, Digital Data MD-920A/G.
TM11-5820-804-20P	Organizational Maintenance Repair Parts and Special Tools List for Modem, Digital Data MD-920A/G.
TM11-5820-804-34P	DS, GS, and Depot Repair Parts and Special Tools List for Modem, Digital Data MD-920A/G.
TM 11-5895-807-13	Operator's, Organizational and Direct Support Maintenance Manual: Encoder-Decoder KY-801/GSC (NSN 5895-01-034-1061).
TM 38-750	The Army Maintenance Management System (TAMMS).
TM 740-90-1	Administrative Storage of Equipment.
TM 750-244-2	Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command).

WIRE LISTS

This appendix contains interconnecting wire run lists for the Synthesizer and Bit Synchronizer card file, A2A1 (table B-1) and Power Supply, A2PS1 (table B-2).

Table B-1. Synthesizer and Bit Synchronizer, Wire List

GENERAL NOTES

I THIS IS A DOUBLE EFTRY TABULAR FORM RUNNING LIST, ALSO KNOWN AS A PIN DICTIONARY. THE SECOND ENTRY CF A WIRE IS INDICATED BY AN ASTERISK (*) FOLLOWING THE WIRE NUMBER EXAMPLE-1708 ANU 178* ARE FIRST AND SECOND ENTRIES CF THE SAME WIRE NUMBER.

2 COLOR CODE ABBREVIATICNS ARE PER USAS Y14.15 AND MIL-STD-12.
BLACK IS BK, BROWN IS BR, RED IS R, ORANGE IS O, YELLOW IS Y,GREEN IS G, BLUE IS BL, VIOLET IS V, GRAY (ALSO CALLED SLATE), IS GY WHITE IS ,.

3 THE FOLLOWING NODE NAMES AND WIRE COLORS ARE STANDARD:
SIGNALS ARE WHITE, RETURNS ARE BLACK, GROUND IS GND AND COLOR BLACK, +5VC IS RED, -5VOC IS YELLOW, +12VDC IS BROWN -12ZVDC IS BLUE +15VDC IS GREEN, -15VDC IS VIOLET, AND +28VDC IS ORANGE. VENDOR ASSEMBLIES WILL NOT BE REWORKED TO MEET THIS REQUIREMENT.

5 MATERIAL IS CALLED OUT ON THE NEXT ASSEMBLY. ITEM ENTRIES ARE FOR REFERENCE ONLY AND THE FOLLOWING ABBREVIATIONS ARE USED. 188 IS RG188A/U. 30SCL IS SOLID AWG 30, INSULATED WIRE WRAP WIRE, E-16 IS INSULATED STRANDED TYPE E WIRE PER MIL-W-16878/4.
STW2 INSICATES SHIELDED TWISTED PAIR. INTERNAL CODING MAY BE SHOWN FOR REF.

6 WHEN 2 OR MORE WIRES ARE INSEPARABLY ASSEMBLED (EXAMPLE COAX AND SHIELDED TWISTED PAIR) THEY ARE GIVEN THE SAME WIRE NU'MER. SHIELD PIGTAILS MUST HAVE SEPARATE WIRE NUMBER.

7 LOWER CASE CHARACTER IS INDICATED BY AN APOSTROPHE FOLLOWING THE LETTER EXAMPLE LOWER CASE A IS A'. A SHIELD COVER IS INDICATED BY A DOLLAR SIGN FOLLOWING THE TERMINAL NAME. EXAMPLE E1$ IS THE SHIELD OVER THE WIRE GOING TO E1.

TERMINATION NOTES
(TERMINATION NOTE NUMBERS MAY NOT BE CONTINUOUS)

1. SOLDER WIRE TO TERMINAL INDICATED IN LIST.

2 CRIPF WIRET COAX CR TWISTED PAIR IN CONTACT PER SM-A-731333 -50 TRU 55 AND INSTALL IN CCNNECTOR PER SM-A-731330-1 THRU 4 AT POSITION GIVEN IN LIST.

6 WRAP AWG 26 OR LAC 30 SOLID WIRE CN .025 SQUARE POST.
6 TURNS MINIMUM CF PARE WIRE AECVE 1.5 TURNS MINIMUM OF INSULATED WIRE ARE REQUIRED. REF MIL-STD-1130. INSLLATICN WRAP MAY BE OMITTED ON TEFLON COVERED WIRE.

			SYNTH & 3IT SYNC I	
	SIZE	CODE IDENT NO.		REV
HIGHEST WIRE KUMEER IS 1070	A	80063	SM-A-759628	F
			SHEET 3	

Table B-1. Synthesizer and Bit Synchronizer, Wire List - Continued

7 SCLDER WIRE TO ..025 SQUARE POST. USE CAUTION TO AVOID DAMAGE TO INSULATION. SOLDER SLEEVE OPTIONAL. IF SOLDER HAS NOT ROUNDED CORNERS OF PCST, WIRE WRAP IS OPTIONAL.

9 CONNECT PIGTAIL TO SHIELD BY USE OF CRIMP OR SOLDER SLEEVE.

10 TERMINATE SHIELD BY CUTTING BACK NEAR TERMINAL. KEEP EXPOSE BRAID SHORT, COVER COUT EDGES WITH HEAT SHRINK SLEEVING.

11 SOLDER BUS-BAR TO TERMINALS INDICATED IN LIST. USE CAUTION TO AVOID DAMAGE TC INSTALLATION.

12 CRIMP 1 OR 2 WIRES IN 1 MS25036 TYPE LUG. BOTH WIRES WILL CARRY THE SAME WIRE NUMBER. DO NOT EXCEED THE CIR-MILL RATING OF THE LOG.

13 TERMINATE COAX IN SMA CONNECTOR. NOTE SHIELD IS CARRIED THRU.

14 ATTACH COAX TO ADAPTER AT BOTH ENDS PER FIGURE 1. PLACE ADAPTERS OVER WIREWRAP PINS AS INDICATED N LIST AND SOLDER. USE CAUTION TO AVOID DAMAGE TO IINSULATION.

15 ATTACH COAX TO ADAPTER AT ONE END PER FIGURE 1. PLACE ADAPTER OVER WIREWRAP PINS AS INDICATED IN LIST AND SOLDER. USE CAUTION TO AVOID DAMAGE TO INSULATION.

Table B-1. Synthesizer and Bit Synchronizer, Wire List - Continued

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
161	ADAPTER	161 14	A1XA11-29	14	188 SHLD	GND	COAX		
161	ADAPTER	161 14	A1XA11-30	14	188 CTR	TVCO	COAX		
161	ADAPTER	161 14	A1XA11-31	14	188 SHLD	GND	COAX		
161	ADAPTER	161 14	A1XA11-65	14	188 SHLD	GND	COAX		
161	ADAPTER	161 14	A1XA11-66	14	188 CTR	TVCO	COAX		
161	ADAPTER	161 14	A1XA11-67	14	188 SHLD	GND	COAX		
161	ADAPTER	161 15	J02-K	2	188 CTR	TVCO	COAX		B
162	ADAPTER	162 14	A1XA11-20	14	188 SHLD	GND	COAX		
162	ADAPTER	162 14	A1XA11-21	14	188 CTR	TVCONT	COAX		
162	ADAPTER	162 14	A1XA11-22	14	188 SHLD	GND	COAX		
162	ADAPTER	162 14	A1XA11-56	14	188 SHLD	GND	COAX		
162	ADAPTER	162 14	A1XA11-57	14	188 CTR	TVCONT	COAX		
162	ADAPTER	162 14	A1XA11-58	14	188 SHLD	GND	COAX		
162	ADAPTER	162 15	J02-P	2	188 CTR	TVCONT	COAX		B
509	ADAPTER	509 14	A1XAC3-31	14	188 SHLD	GND	COAX		
509	ADAPTER	509 14	A1XAC3-32	14	188 CTR	TSC45M	COAX		
509	ADAPTER	509 14	A1XAC3-33	14	188 SHLD	GND	COAX		
509	ADAPTER	509 14	A1XAC3-67	14	188 SHLD	GND	COAX		
509	ADAPTER	509 14	A1XAC3-68	14	188 CTR	TSC45M	COAX		
509	ADAPTER	509 14	A1XAC3-69	14	188 SHLD	GND	COAX		
509	ADAPTER	509 14	A1XA12-27	14	188 SHLD	GND	COAX		
509	ADAPTER	509 14	A1XA12-28	14	188 CTR	TSC45M	COAX		
509	ADAPTER	509 14	A1XA12-29	14	188 SHLD	GND	COAX		
509	ADAPTER	509 14	A1XA12-63	14	188 SHLD	GND	COAX		
509	ADAPTER	509 14	A1XA12-64	14	188 CTR	TSC45M	COAX		
509	ADAPTER	509 14	A1XA12-65	14	188 SHLD	GND	COAX		
510	ADAPTER	510 14	A1XAC3-06	14	188 SHLD	GND	COAX		
510	ADAPTER	510 14	A1XAC3-07	14	188 CTR	TM1X0	COAX		
510	ADAPTER	510 14	A1XAC3-08	14	188 SHLD	GND	COAX		
510	ADAPTER	510 14	A1XAC3-42	14	188 SHLD	GND	COAX		
510	ADAPTER	510 14	A1XAC3-43	14	188 CTR	TM1X0	COAX		
510	ADAPTER	510 14	A1XAC3-44	14	188 SHLD	GND	COAX		
510	ADAPTER	510 14	A1XA10-02	14	188 SHLD	GND	COAX		
510	ADAPTER	510 14	A1XA10-03	14	188 CTR	TM1X0	COAX		
510	ADAPTER	510 14	A1XA10-04	14	188 SHLD	GND	COAX		
510	ADAPTER	510 14	A1XA10-38	14	188 SHLD	GND	COAX		
510	ADAPTER	510 14	A1XA10-39	14	188 CTR	TM1X0	COAX		
510	ADAPTER	510 14	A1XA10-40	14	188 SHLD	GND	COAX		
536	ADAPTER	536 14	A1XAC6-29	14	188 SHLD	GND	COAX		
536	ADAPTER	536 14	A1XAC6-30	14	188 CTR	T45MVCO	COAX		

WIRE NO.	FROM END	FROM TERM	FROM ENC	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
536	ADAPTER	536	14 A1XAC6-31	14	188 SHLD	GND	COAX		
536	ADAPTER	536	14 A1XAC6-65	14	188 SHLD	GND	COAX		
536	ADAPTER	536	14 A1XAC6-66	14	188 CTR	T45MVCO	COAX		
536	ADAPTER	536	14 A1XAC6-67	14	188 SHLD	GND	COAX		
536	ADAPTER	536	14 A1XAC8-29	14	188 SHLD	GND	COAX		
536	ADAPTER	536	14 A1XAC8-30	14	188 CTR	T45MVCO	COAX		
536	ADAPTER	536	14 A1XAC8-31	14	188 SHLD	GND	COAX		
536	ADAPTER	536	14 A1XAC8-65	14	188 SHLD	GND	COAX		
536	ADAPTER	536	14 A1XAC8-66	14	188 CTR	T45MVCO	COAX		
536	ADAPTER	536	14 A1XAC8-67	14	188 SHLD	GND	COAX		
543	ADAPTER	543	14 A1XAC8-09	14	188 SHLD	GND	COAX		
543	ADAPTER	543	14 A1XAC8-10	14	188 CTR	TSCTCXO	COAX		
543	ADAPTER	543	14 A1XAC8-11	14	188 SHLD	GND	COAX		
543	ADAPTER	543	14 A1XAC8-45	14	188 SHLD	GND	COAX		
543	ADAPTER	543	14 A1XAC8-46	14	188 CTR	TSCTCXO	COAX		
543	ADAPTER	543	14 A1XAC8-47	14	188 SHLD	GND	COAX		
543	ADAPTER	543	14 A1XA12-10	14	188 SHLD	GND	COAX		
543	ADAPTER	543	14 A1XA12-11	14	188 CTR	TSCTCXO	COAX		
543	ADAPTER	543	14 A1XA12-12	14	188 SHLD	GND	COAX		
543	ADAPTER	543	14 A1XA12-46	14	188 SHLD	GND	COAX		
543	ADAPTER	543	14 A1XA12-47	14	188 CTR	TSCTCXO	COAX		
543	ADAPTER	543	14 A1XA12-48	14	188 SHLD	GND	COAX		
544	ADAPTER	544	14 A1XAC8-21	14	188 SHLD	GND	COAX		
544	ADAPTER	544	14 A1XAC8-22	14	188 CTR	T45M1X	COAX		
544	ADAPTER	544	14 A1XAC8-23	14	188 SHLD	GND	COAX		
544	ADAPTER	544	14 A1XAC8-57	14	188 SHLD	GND	COAX		
544	ADAPTER	544	14 A1XAC8-58	14	188 CTR	T45M1X	COAX		
544	ADAPTER	544	14 A1XAC8-59	14	188 SHLD	GND	COAX		
544	ADAPTER	544	14 A1XA10-08	14	188 SHLD	GND	COAX		
544	ADAPTER	544	14 A1XA10-09	14	188 CTR	T45M1X	COAX		
544	ADAPTER	544	14 A1XA10-10	14	188 SHLD	GND	COAX		
544	ADAPTER	544	14 A1XA10-44	14	188 SHLD	GND	COAX		
544	ADAPTER	544	14 A1XA10-45	14	188 CTR	T45M1X	COAX		
544	ADAPTER	544	14 A1XA10-46	14	188 SHLD	GND	COAX		
545	ADAPTER	545	14 A1XAC2-07	14	188 SHLD	GND	COAX		
545	ADAPTER	545	14 A1XAC2-08	14	188 CTR	T45MA	COAX		
545	ADAPTER	545	14 A1XAC2-09	14	188 SHLD	GND	COAX		
545	ADAPTER	545	14 A1XAC2-43	14	188 SHLD	GND	COAX		
545	ADAPTER	545	14 A1XAC2-44	14	188 CTR	T45MA	COAX		
545	ADAPTER	545	14 A1XAC2-45	14	188 SHLD	GND	COAX		

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1070 A 80063 SM-A-759628 F

SHEET 6

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
545	ADAPTER	545 14	A1XAC8-12	14	188 SHLD	GND	COAX		
545	ADAPTER	545 14	A1XAC8-13	14	188 CTR	T45MA	COAX		
545	ADAPTER	545 14	A1XAC8-14	14	188 SHLD	GND	COAX		
545	ADAPTER	545 14	A1XAC8-48	14	188 SHLD	GND	COAX		
545	ADAPTER	545 14	A1XAC8-49	14	188 CTR	T45MA	COAX		
545	ADAPTER	545 14	A1XAC8-50	14	188 SHLD	GND	COAX		
551	ADAPTER	551 14	A1XA1C-C5	14	188 SHLD	GND	COAX		
551	ADAPTER	551 14	A1XA1C-C6	14	188 CTR	R15M1X	COAX		
551	ADAPTER	551 14	A1XA1C-C7	14	188 SHLD	GND	COAX		
551	ADAPTER	551 14	A1XA10-41	14	188 SHLD	GND	COAX		
551	ADAPTER	551 14	A1XA1C-42	14	188 CTR	R15M1X	COAX		
551	ADAPTER	551 14	A1XA10-43	14	188 SHLD	GND	COAX		
551	ADAPTER	551 14	A1XA11-15	14	188 SHLD	GND	COAX		
551	ADAPTER	551 14	A1XA11-16	14	188 CTR	R15M1X	COAX		
551	ADAPTER	551 14	A1XA11-17	14	188 SHLD	GND	COAX		
551	ADAPTER	551 14	A1XA11-51	14	188 SHLD	GND	COAX		
551	ADAPTER	551 14	A1XA11-52	14	188 CTR	R15M1X	COAX		
551	ADAPTER	551 14	A1XA11-53	14	188 SHLD	GND	COAX		
860	ADAPTER	860 15	A2XA14-29	15	188 SHLD	GND	COAX		
860	ADAPTER	860 15	A2XA14-30	15	188 CTR	RVCO	COAX		
860	ADAPTER	860 15	A2XA14-31	15	188 SHLD	GND	COAX		
860	ADAPTER	860 15	A2XA14-65	15	188 SHLD	GND	COAX		
860	ADAPTER	860 15	A2XA14-66	15	188 CTR	RVCO	COAX		
860	ADAPTER	860 15	A2XA14-67	15	188 SHLD	GND	COAX		
860	ADAPTER	860 15	J02-B	2	188 CTR	RVCO	COAX		
861	ADAPTER	861 15	A2XA14-20	15	188 SHLD	GND	COAX		
861	ADAPTER	861 15	A2XA14-21	15	188 CTR	RVCONT	COAX		
861	ADAPTER	861 15	A2XA14-22	15	188 SHLD	GND	COAX		
861	ADAPTER	861 15	A2XA14-56	15	188 SHLD	GND	COAX		
861	ADAPTER	861 15	A2XA14-57	15	188 CTR	RVCONT	COAX		
861	ADAPTER	861 15	A2XA14-58	15	188 SHLD	GND	COAX		
861	ADAPTER	861 15	J02-H	2	188 CTR	RVCONT	COAX		
902	ADAPTER	902 14	A2XA16-29	14	188 SHLD	GND	COAX		
902	ADAPTER	902 14	A2XA16-30	14	188 CTR	R45MVCO	COAX		
902	ADAPTER	902 14	A2XA16-31	14	188 SHLD	GND	COAX		
902	ADAPTER	902 14	A2XA16-65	14	188 SHLD	GND	COAX		
902	ADAPTER	902 14	A2XA16-66	14	188 CTR	R45MVCO	COAX		
902	ADAPTER	902 14	A2XA16-67	14	188 SHLD	GND	COAX		
902	ADAPTER	902 14	A2XA18-29	14	188 SHLD	GND	COAX		
902	ADAPTER	902 14	A2XA16-30	14	188 CTR	R45MVCO	COAX		

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR	ITEM	REF NODE	NOTE	REMARKS	REV
S02	ADAPTER	902	14 A2XA16-31	14	188	SHLD	GND	COAX		
S02	ADAPTER	902	14 A2XA16-65	14	188	SHLD	GND	COAX		B
S02	ADAPTER	902	14 A2XA16-66	14	188	CTR	R45MVCO	COAX		B
S02	ADAPTER	902	14 A2XA16-67	14	188	SHLD	GND	COAX		
903	ADAPTER	903	14 A2XA15-C2	14	188	SHLD	GND	COAX		
S03	ADAPTER	903	14 A2XA15-C3	14	188	CTR	RM1XO	COAX		
903	ADAPTER	903	14 A2XA15-C4	14	188	SHLD	GND	COAX		
903	ADAPTER	903	14 A2XA15-38	14	188	SHLD	GND	COAX		
903	ADAPTER	903	14 A2XA15-39	14	188	CTR	RM1XO	COAX		
S03	ADAPTER	903	14 A2XA15-40	14	188	SHLD	GND	COAX		
903	ADAPTER	903	14 A2XA21-C6	14	188	SHLD	GND	COAX		
903	ADAPTER	903	14 A2XA21-C7	14	188	CTR	RM1XO	COAX		
903	ADAPTER	903	14 A2XA21-C8	14	188	SHLD	GND	COAX		
S03	ADAPTER	903	14 A2XA21-42	14	188	SHLD	GND	COAX		
903	ADAPTER	903	14 A2XA21-43	14	188	CTR	RM1XO	COAX		
S03	ADAPTER	903	14 A2XA21-44	14	188	SHLD	GND	COAX		
S04	ADAPTER	904	14 A2XA15-C8	14	188	SHLD	GND	COAX		
S04	ADAPTER	904	14 A2XA15-C9	14	188	CTR	R45M1X	COAX		
904	ADAPTER	904	14 A2XA15-10	14	188	SHLD	GND	COAX		
904	ADAPTER	904	14 A2XA15-44	14	188	SHLD	GND	COAX		
904	ADAPTER	904	14 A2XA15-45	14	188	CTR	R45M1X	COAX		
904	ADAPTER	904	14 A2XA15-46	14	188	SHLD	GND	COAX		
904	ADAPTER	904	14 A2XA16-21	14	188	SHLD	GND	COAX		
904	ADAPTER	904	14 A2XA16-22	14	188	CTR	R45M1X	COAX		
904	ADAPTER	904	14 A2XA16-23	14	188	SHLD	GND	COAX		
S04	ADAPTER	904	14 A2XA16-57	14	188	SHLD	GND	COAX		
S04	ADAPTER	904	14 A2XA16-58	14	188	CTR	R45M1X	COAX		
904	ADAPTER	904	14 A2XA16-59	14	188	SHLD	GND	COAX		
909	ADAPTER	909	14 A2XA16-12	14	188	SHLD	GND	COAX		
S09	ADAPTER	909	14 A2XA16-13	14	188	CTR	R45MA	COAX		
S09	ADAPTER	909	14 A2XA16-14	14	188	SHLD	GND	COAX		
909	ADAPTER	909	14 A2XA16-48	14	188	SHLD	GND	COAX		
S09	ADAPTER	909	14 A2XA16-49	14	188	CTR	R45MA	COAX		
909	ADAPTER	909	14 A2XA16-50	14	188	SHLD	GND	COAX		
909	ADAPTER	909	14 A2XA23-C7	14	188	SHLD	GND	COAX		
S09	ADAPTER	909	14 A2XA23-C8	14	188	CTR	R45MA	COAX		
909	ADAPTER	909	14 A2XA23-C9	14	188	SHLD	GND	COAX		
S09	ADAPTER	909	14 A2XA23-43	14	188	SHLD	GND	COAX		
909	ADAPTER	909	14 A2XA23-44	14	188	CTR	R45MA	COAX		
S09	ADAPTER	909	14 A2XA23-45	14	188	SHLD	GND	COAX		

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
947	ADAPTER	947 14	A2XA14-15	14	188 SHLD	GND	COAX		
947	ADAPTER	947 14	A2XA14-16	14	188 CTR	R15M1X	COAX		
947	ADAPTER	947 14	A2XA14-17	14	188 SHLD	GND	COAX		
947	ADAPTER	947 14	A2XA14-51	14	188 SHLD	GND	COAX		
947	ADAPTER	947 14	A2XA14-52	14	188 CTR	R15M1X	COAX		
947	ADAPTER	947 14	A2XA14-53	14	188 SHLD	GND	COAX		
947	ADAPTER	947 14	A2XA15-05	14	188 SHLD	GND	COAX		
947	ADAPTER	947 14	A2XA15-06	14	188 CTR	R15M1X	COAX		
947	ADAPTER	947 14	A2XA15-07	14	188 SHLD	GND	COAX		
947	ADAPTER	947 14	A2XA15-41	14	188 SHLD	GND	COAX		
947	ADAPTER	947 14	A2XA15-42	14	188 CTR	R15M1X	COAX		
947	ADAPTER	947 14	A2XA15-43	14	188 SHLD	GND	COAX		
1037	ADAPTER	1037 15	A2XAC1-01	15	188 SHLD	GND	COAX		B
1037	ADAPTER	1037 15	A2XAC1-02	15	188 CTR	LOSINB+	COAX		B
1037	ADAPTER	1037 15	A2XAC1-03	15	188 SHLD	GND	COAX		B
1037	ADAPTER	1037 15	A2XAC1-37	15	188 SHLD	GND	COAX		B
1037	ADAPTER	1037 15	A2XAC1-38	15	188 CTR	LOSINB+	COAX		B
1037	ADAPTER	1037 15	A2XAC1-39	15	188 SHLD	GND	COAX		B
1037	ADAPTER	1037 15	P01-CTR	13	188 CTR	LOSINB+	COAX		B
1037	ADAPTER	1037 15	P01-SHELL	13	188 SHLD	GND	COAX		B
111	A1XA01-C2	1	A1JC2-20	6	E-20 R	+5VDC			B
1003	A1J01-01	6	A1J01-21	16	30SCL BK	GND			B
1048	A1J01-01	6	A1JC2-40	6	26SOL BK	GND			B
190	A1J01-01	7	W1-	12	E-24 BK	GND			
277	A1J01-C3	6	A2XAC6-15	6	30SCL W	NOENCC			
278	A1J01-C4	6	A2XAC6-10	6	30SCL W	EXTENCC			
279	A1J01-C5	6	A2XAC4-13	6	30SCL W	ENOPERC			
281	A1J01-C7	6	A2XAC4-14	6	30SCL W	ENTESTC			
283	A1J01-C9	6	A2XAC6-59	6	30SCL W	NODECC			
284	A1J01-10	6	A2XAC6-48	6	30SCL W	EXTDECC			
138	A1J01-11	6	A2XAC7-27	6	30SCL W	TSTSEQ			
139	A1J01-12	6	A2XAC7-62	6	30SCL W	TSTTXBS			
287	A1J01-13	6	A2XAC7-63	6	30SCL W	TSTRXBS			
141	A1J01-15	6	A2XAC7-65	6	30SCL W	TSTALT			
964	A1J01-16	6	A1JC1-18	6	30SCL BK	GND			B
1047	A1J01-16	6	A1XAC1-01	6	30SCL BK	GND			B
965	A1J01-17	6	A2XAC1-25	6	30SOL W	IGFRLYE			B
964*	A1J01-18	6	A1JC1-16	6	30SCL BK	GND			B
291	A1J01-19	6	A2XAC8-30	6	30SCL W	ERRCNT			
1003*	A1J01-21	16	A1JC1-01	6	30SCL BK	GND			B

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1070 A 80063 SM-A-759628 F

SHEET 9

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
294	A1J01-22	6	A2XAC9-11	6	30SOL W	TESTP5V			
295	A1J01-23	6	A2XAC9-49	6	30SOL W	TESTM5V			
296	A1J01-24	6	A2XAC9-52	6	30SOL W	TESTP15			
297	A1J01-25	6	A2XAC9-16	6	30SOL W	TESTM15			
1008	A1J01-26	6	A2XAC9-C8	6	30SOL W	ERRSIG	TW2-1008		B
1008	A1J01-27	6	A2XAC9-C9	6	30SOL BK	ERRGND	TW2-1008		B
299	A1J01-28	6	A1XAC6-25	6	30SOL W	TSYNTST			
402	A1J01-29	6	A2XAC6-52	6	30SOL W	MANSMPC			
254	A1J01-30	6	A2XAC8-50	6	30SOL W	CMPATOC			
274	A1J01-31	6	A2XAC8-33	6	30SOL W	ERRCUT	TW2-274		
274	A1J01-32	6	A2XAC6-28	6	30SOL BK	ERRGND	TW2-274		
405	A1J01-33	6	A2XAC7-13	6	30SOL W	SYNCN11	TW2-405		
405	A1J01-34	6	A2XAC7-37	6	30SOL BK	SYNCGND	TW2-405		
406	A1J01-35	6	A2XAC7-52	6	30SOL W	COMPCKC	TW2-406		
406	A1J01-36	6	A2XAC7-37	6	30SOL BK	COMPGND	TW2-406		
1014	A1J01-37	6	A2XA18-25	6	30SOL W	RSYNTST	TW2-1014		B
1014	A1J01-38	6	A2XA18-20	6	30SOL BK	RSYNGND	TW2-859		B
62	A1J02-01	6	A1J02-40	6	26SOL BK	GND			B
61	A1J02-01	6	A1J03-01	6	26SOL BK	GND			B
166	A1J02-02	6	A2XAC6-22	6	30SOL W	DIFENCC			
167	A1J02-03	6	A2XAC6-14	6	30SOL W	DIFDECT			
169	A1J02-05	6	A2XAC4-15	6	30SOL W	ENCLKRC			
676	A1J02-06	6	A2XA04-16	6	30SOL W	ENSTDRC			
1029	A1J02-07	6	A2XA1C-45	6	30SOL W	AUCALM1			B
766	A1J02-08	6	A2XA1C-47	6	30SOL W	AUDAL42			
1052	A1J02-09	6	A1J02-18	6	30SOL R	+5VDC			
756	A1J02-10	6	A2XA1C-52	6	30SOL W	ALMRST			
175	A1J02-11	6	A2XA10-46	6	30SOL W	THERMO			
59	A1J02-12	6	A1J02-18	6	30SOL R	+5VDC			
67	A1J02-12	6	A1J02-22	6	30SOL R	+5VDC			
178	A1J02-17	6	A2XA1C-12	6	30SOL W	RXBSLOL			
1052*	A1J02-18	6	A1J02-09	6	30SOL R	+5VDC			
59*	A1J02-18	6	A1J02-12	6	30SOL R	+5VDC			
1	A1J02-18	6	A1J02-20	7	30SOL R	+5VDC			
111*	A1J02-20	6	A1XAC1-02	1	E-20 R	+5VDC			B
1*	A1J02-20	7	A1J02-18	6	30SOL R	+5VDC			
180	A1J02-21	6	A2XA1C-22	6	30SOL W	RXFAIL			
67*	A1J02-22	6	A1J02-12	6	30SOL R	+5VDC			
80	A1J02-22	6	A1J02-24	6	30SOL R	+5VDC			
181	A1J02-23	6	A2XA1C-09	6	30SOL W	TXBSFL			

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1070 A 80C63 SM-A-759628 F

SHEET 10

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
80*	A1J02-24	6	A1J02-22	6	30SCL R	+5VDC			
91	A1J02-24	6	A1J02-30	6	30SCL R	+5VDC			
566	A1J02-27	6	A2XA10-03	6	30SCL W	TXFAIL			B
567	A1J02-28	6	A1J02-30	6	30SCL R	+5VDC			B
91*	A1J02-30	6	A1J02-24	6	30SCL R	+5VDC			
567*	A1J02-30	6	A1JC2-28	6	30SCL R	+5VDC			B
92	A1J02-30	6	A1JC2-38	6	30SCL R	+5VDC			
312	A1J02-31	6	A2XAC9-51	6	30SCL W	CLKZER			
110	A1J02-32	6	A1J02-34	6	30SCL R	+5VDC			
314	A1J02-33	6	A2XAC9-57	6	30SCL W	CLKONE			
110*	A1J02-34	6	A1J02-32	6	30SCL R	+5VDC			
108	A1J02-34	6	A1JC2-36	6	30SCL R	+5VDC			
187	A1J02-35	6	A2XAC9-14	6	30SCL W	DATZER			
108*	A1J02-36	6	A1JC2-34	6	30SCL R	+5VDC			
107	A1J02-36	6	A1JC2-38	6	30SCL R	+5VDC			
188	A1J02-37	6	A2XAC9-50	6	30SCL W	DATONE			
92*	A1J02-38	6	A1J02-30	6	30SCL R	+5VDC			
107*	A1J02-38	6	A1JC2-36	6	30SCL R	+5VDC			
1048*	A1J02-40	6	A1J01-01	6	26SCL BK	GND			B
62*	A1JC2-40	6	A1J02-01	6	26SCL BK	GND			B
61*	A1J03-01	6	A1JC2-01	6	26SCL BK	GND			B
290	A1J03-01	6	A1J03-11	6	26SOL BK	GND			
1021	A1J03-02	6	A2XA24-02	7	30SCL R	+5VDC			B
908	A1J03-03	6	A2XA23-03	6	30SCL W	R10-100K			
1002	A1J03-04	6	A2XA23-06	6	30SCL W	R1-10M			B
1001	A1J03-05	6	A2XA23-05	6	30SCL W	R100K-1M			B
841	A1J03-06	6	A2XA24-14	6	30SOL W	R0-COM			
938	A1J03-07	6	A2XA24-65	6	30SCL W	RX9-0-1			
939	A1J03-08	6	A2XA24-25	6	30SOL W	RX9-0-2			
940	A1J03-09	6	A2XA24-27	6	30SCL W	RX9-0-4			
941	A1JC3-10	6	A2XA24-66	6	30SCL W	RX9-0-8			
290*	A1J03-11	6	A1JC3-01	6	26SCL BK	GND			
942	A1J03-12	6	A2XA24-15	6	30SOL W	R1-COM			
942	A1J03-13	6	A2XA24-69	6	30SCL W	RX9-1-1			
943	A1JC3-14	6	A2XA24-30	6	30SCL W	RX9-1-2			
944	A1J03-15	6	A2XA24-63	6	30SCL W	RX9-1-4			
945	A1J03-16	6	A2XA24-68	6	30SCL W	RX9-1-8			
843	A1J03-17	6	A2XA24-23	6	30SCL W	R2-COM			
869	A1JC3-18	6	A2XA24-41	6	30SCL W	RX9-2-1			
870	A1J03-19	6	A2XA24-C8	6	30SCL W	RX9-2-2			

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1070 A 80063 SM-A-759628 F

SHEET 11

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
646	A1J03-20	6	A2XA24-44	6	30SCL W	RX9-2-4			
871	A1J03-21	6	A2XA24-42	6	30SCL W	RX9-2-8			
644	A1J03-23	6	A2XA24-51	6	30SCL W	R3-COM			
873	A1J03-24	6	A2XA24-05	6	30SCL W	RX9-3-1			
874	A1J03-25	6	A2XA24-43	6	30SCL W	RX9-3-2			
875	A1J03-26	6	A2XA24-54	6	30SCL W	RX9-3-4			
876	A1J03-27	6	A2XA24-56	6	30SCL W	RX9-3-8			
845	A1J03-33	6	A2XA24-52	6	30SCL W	R4-COM			
877	A1J03-34	6	A2XA24-58	6	30SCL W	RX9-4-1			
878	A1J03-35	6	A2XA24-47	6	30SCL W	RX9-4-2			
879	A1J03-36	6	A2XA24-10	6	30SCL W	RX9-4-4			
880	A1J03-37	6	A2XA24-22	6	30SCL W	RX9-4-8			
1047*	A1XA01-01	6	A1JC1-16	6	30SCL BK	GND			B
3	A1XA01-C1	11	BUS-3	11	BUS	GND			
8	A1XA01-C2	11	BUS-8	11	BUS	+5VDC			
626	A1XA01-C3	6	A1XAC2-65	6	30SCL W	TXPD3-1			
22	A1XA01-C5	6	A2J01-24	6	30SCL W	TX9-3-1			
625	A1XA01-C6	6	A1XAC2-69	6	30SCL W	TXPD2-8			
623	A1XA01-C7	6	A1XAC2-32	6	30SCL W	TXPD2-2			
19	A1XAC1-C8	6	A2J01-19	6	30SCL W	TX9-2-2			
624	A1XA01-C9	6	A1XAC2-68	6	30SCL W	TXPD2-4			
30	A1XA01-10	6	A2J01-36	6	30SCL W	TX9-4-4			
631	A1XA01-11	6	A1XAC2-60	6	30SCL W	TXPD4-2			
582	A1XA01-12	6	A1XAC2-33	6	30SCL W	TLOPGM			
628	A1XAC1-13	6	A1XAC2-66	6	30SCL W	TXPD3-4			
6	A1XA01-14	6	A2J01-06	6	30SCL W	T0-COM			
12	A1XA01-15	6	A2JC1-12	6	30SOL W	T1-COM			
633	A1XA01-21	6	A1XA02-61	6	30SCL W	TXPD4-8			
31	A1XA01-22	6	A2JC1-37	6	30SOL W	TX9-4-8			
17	A1XA01-23	6	A2JC1-17	6	30SCL W	T2-COM			
611	A1XA01-24	6	A1XAC5-12	6	30SCL W	TXMX4			
639	A1XA01-25	6	A2JC1-C8	6	30SCL W	TX9-0-2			
615	A1XA01-26	6	A1XAC2-14	6	30SCL W	TXPD0-2			
9	A1XA01-27	6	A2J01-09	6	30SCL W	TX9-0-4			
619	A1XA01-28	6	A1XAC2-63	6	30SCL W	TXPD1-2			
635	A1XA01-29	6	A1XAC2-23	6	30SCL W	TXPD5-2			
14	A1XA01-30	6	A2J01-14	6	30SOL W	TX9-1-2			
614	A1XA01-31	6	A1XAC2-57	6	30SCL W	TXPD0-1			
621	A1XA01-32	6	A1XAC2-62	6	30SCL W	TXPD1-8			
618	A1XA01-33	6	A1XAC2-28	6	30SCL W	TXPD1-1			

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1070 A 80063 SM-A-759628 F

SHEET 12

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
634	A1XA01-35	6	A1XAC2-59	6	30SCL W	TXPD5-1			
3	A1XA01-37	11	BUS-3	11	BUS	GND			
8	A1XA01-38	11	BUS-8	11	BUS	+5VDC			
622	A1XA01-39	6	A1XAC2-67	6	30SCL W	TXPD2-1			
18	A1XA01-41	6	A2JC1-18	6	30SOL W	TX9-2-1			
26	A1XA01-42	6	A2JC1-21	6	30SCL W	TX9-2-8			
23	A1XA01-43	6	A2JC1-25	6	30SCL W	TX9-3-2			
20	A1XA01-44	6	A2JC1-20	6	30SCL W	TX9-2-4			
627	A1XA01-45	6	A1XAC2-30	6	30SCL W	TXPD3-2			
613	A1XA01-46	6	A1XAC5-11	6	30SOL W	TXMX1			
29	A1XA01-47	6	A2JC1-35	6	30SCL W	TX9-4-2			
632	A1XA01-48	6	A1XAC2-25	6	30SCL W	TXPD4-4			
21	A1XA01-51	6	A2JC1-23	6	30SCL W	T3-COM			
27	A1XA01-52	6	A2J01-33	6	30SCL W	T4-COM			
24	A1XA01-54	6	A2JC1-26	6	30SCL W	TX9-3-4			
629	A1XA01-55	6	A1XAC2-31	6	30SCL W	TXPD3-8			
25	A1XA01-56	6	A2J01-27	6	30SCL W	TX9-3-8			
630	A1XA01-57	6	A1XA02-24	6	30SCL W	TXPD4-1			
28	A1XA01-58	6	A2JC1-34	6	30SCL W	TX9-4-1			
610	A1XA01-59	6	A1XAC5-15	6	30SCL W	TXMX8			
612	A1XA01-60	6	A1XAC5-14	6	30SCL W	TXMX2			
636	A1XA01-61	6	A1XAC2-58	6	30SCL W	TXPD5-4			
616	A1XA01-62	6	A1XAC2-15	6	30SCL W	TXPD0-4			
15	A1XA01-63	6	A2JC1-15	6	30SOL W	TX9-1-4			
620	A1XA01-64	6	A1XA02-27	6	30SCL W	TXPD1-4			
7	A1XA01-65	6	A2J01-07	6	30SCL W	TX9-0-1			
10	A1XA01-66	6	A2JC1-10	6	30SCL W	TX9-0-8			
617	A1XA01-67	6	A1XAC2-16	6	30SCL W	TXPD0-8			
16	A1XA01-68	6	A2JC1-16	6	30SCL W	TX9-1-8			
13	A1XA01-69	6	A2J01-13	6	30SCL W	TX9-1-1			
637	A1XA01-71	6	A1XAC2-22	6	30SCL W	TXPD5-8			
3	A1XA02-C1	11	BUS-3	11	BUS	GND			
8	A1XA02-C2	11	BUS-8	11	BUS	+5VDC			
575	A1XA02-C3	6	A2JC1-03	6	30SCL W	T10-100K			
1010	A1XA02-C5	6	A2JC1-C5	6	30SOL W	T100K-1M			B
1011	A1XA02-C6	6	A2JC1-C4	6	30SCL W	T1-10M			B
545*	A1XA02-C7	14	ADAPTER 545	14	188 SHLD	GND	COAX		
545*	A1XA02-C8	14	ADAPTER 545	14	188 CTR	T45MA	COAX		
545*	A1XA02-C9	14	ADAPTER 545	14	188 SHLD	GND	COAX		
615*	A1XA02-14	6	A1XAC1-26	6	30SCL W	TXPD0-2			

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1070 A 80063 SM-A-759628 F

SHEET 13

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
616*	A1XA02-15	6	A1XA01-62	6	30SCL W	TXPD0-4			
617*	A1XA02-16	6	A1XAC1-67	6	30SCL W	TXPD0-8			
637*	A1XA02-22	6	A1XA01-71	6	30SCL W	TXPD5-8			
635*	A1XA02-23	6	A1XA01-29	6	30SCL W	TXPD5-2			
630*	A1XA02-24	6	A1XAC1-57	6	30SCL W	TXPD4-1			
632*	A1XA02-25	6	A1XAC1-48	6	30SCL W	TXPD4-4			
620*	A1XA02-27	6	A1XAC1-64	6	30SCL W	TXPD1-4			
618*	A1XA02-28	6	A1XAC1-33	6	30SCL W	TXPD1-1			
627*	A1XA02-30	6	A1XAC1-45	6	30SCL W	TXPD3-2			
629*	A1XA02-31	6	A1XAC1-55	6	30SCL W	TXPD3-8			
623*	A1XA02-32	6	A1XAC1-67	6	30SCL W	TXPD2-2			
582*	A1XA02-33	6	A1XAC1-12	6	30SCL W	TLDPGM			
581	A1XA02-35	6	A1XAC6-21	6	30SCL W	TSAMP			
3	A1XA02-37	11	BUS-3	11	BUS	GND			
8	A1XA02-38	11	BUS-8	11	BUS	+5VDC			
576	A1XA02-39	6	A1XAC5-27	6	30SCL W	T10100KT			
578	A1XA02-41	6	A1XAC5-30	6	30SCL W	T100K1MT			
580	A1XA02-42	6	A1XAC5-31	6	30SCL W	T1-10MT			
545*	A1XA02-43	14	ADAPTER 545	14	188 SHLD	GND	COAX		
545*	A1XA02-44	14	ADAPTER 545	14	188 CTR	T45MA	COAX		
545*	A1XA02-45	14	ADAPTER 545	14	188 SHLD	GND	COAX		
614*	A1XA02-57	6	A1XA01-31	6	30SCL W	TXPD0-1			
636*	A1XA02-58	6	A1XAC1-61	6	30SCL W	TXPD5-4			
634*	A1XA02-59	6	A1XAC1-35	6	30SCL W	TXPD5-1			
631*	A1XA02-60	6	A1XA01-11	6	30SCL W	TXPD4-2			
633*	A1XA02-61	6	A1XAC1-21	6	30SCL W	TXPD4-8			
621*	A1XA02-62	6	A1XA01-32	6	30SCL W	TXPD1-8			
619*	A1XA02-63	6	A1XA01-28	6	30SCL W	TXPD1-2			
626*	A1XA02-65	6	A1XA01-03	6	30SCL W	TXPD3-1			
628*	A1XA02-66	6	A1XA01-13	6	30SCL W	TXPD3-4			
622*	A1XA02-67	6	A1XAC1-39	6	30SCL W	TXPD2-1			
624*	A1XA02-68	6	A1XAC1-09	6	30SCL W	TXPD2-4			
625*	A1XA02-69	6	A1XA01-06	6	30SCL W	TXPD2-8			
8	A1XA03-02	11	BUS-8	11	BUS	+5VDC			
568	A1XAC3-04	11	BUS-568	11	BUS	-5VDC			B
510*	A1XAC3-06	14	ADAPTER 510	14	188 SHLD	GND	COAX		
510*	A1XA03-07	14	ADAPTER 510	14	188 CTR	TM1XO	COAX		
510*	A1XA03-08	14	ADAPTER 510	14	188 SHLD	GND	COAX		
512	A1XA03-14	6	A1XAC5-28	6	30SCL W	TM1XD	TW2-512		
512	A1XA03-15	6	A1XAC5-29	6	30SCL BK	TM1XDGND	TW2-512		

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
51	A1XA03-17	11	BUS-51	11	BUS	GND			B
52	A1XA03-18	11	BUS-52	11	BUS	GND			B
55	A1XA03-19	11	BUS-55	11	BUS	GND			B
511	A1XA03-20	6	A1XAC5-01	6	30SCL BK	TTXLOGND	TW2-511		
53	A1XA03-20	11	BUS-53	11	BUS	GND			B
511	A1XA03-21	6	A1XAC5-C7	6	30SCL W	TTXLO	TW2-511		
509*	A1XA03-31	14	ADAPTER 509	14	188 SHLD	GND	COAX		
5C9*	A1XA03-32	14	ADAPTER 5C9	14	188 CTR	TSC45M	COAX		
5C9*	A1XA03-33	14	ADAPTER 509	14	188 SHLD	GND	COAX		
318	A1XA03-36	11	BUS-318	11	BUS	+15VDC			
8	A1XA03-38	11	BUS-8	11	BUS	+5VDC			
568	A1XA03-40	11	BUS-568	11	BUS	-5VDC			B
510*	A1XA03-42	14	ADAPTER 510	14	188 SHLD	GND	COAX		
510*	A1XA03-43	14	ADAPTER 51C	14	188 CTR	TM1XO	COAX		
510*	A1XA03-44	14	ADAPTER 510	14	188 SHLD	GND	COAX		
51	A1XA03-53	11	BUS-51	11	BUS	GND			B
52	A1XA03-54	11	BUS-52	11	BUS	GND			B
55	A1XA03-55	11	BUS-55	11	BUS	GND			B
53	A1XA03-56	11	BUS-53	11	BUS	GND			B
509*	A1XA03-67	14	ADAPTER 509	14	188 SHLD	GND	COAX		
509*	A1XA03-68	14	ADAPTER 509	14	188 CTR	TSC45M	COAX		
5C9*	A1XA03-69	14	ADAPTER 5C9	14	188 SHLD	GND	COAX		
318	A1XA03-72	11	BUS-318	11	BUS	+15VDC			
8	A1XA04-C2	11	BUS-8	11	BUS	+5VDC			B
51	A1XAC4-17	11	BUS-51	11	BUS	GND			B
52	A1XAC4-18	11	BUS-52	11	BUS	GND			B
55	A1XAC4-19	11	BUS-55	11	BUS	GND			B
53	A1XAC4-20	11	BUS-53	11	BUS	GND			B
318	A1XA04-36	11	BUS-318	11	BUS	+15VDC			B
8	A1XA04-38	11	BUS-8	11	BUS	+5VDC			B
51	A1XAC4-53	11	BUS-51	11	BUS	GND			B
52	A1XA04-54	11	BUS-52	11	BUS	GND			B
55	A1XAC4-55	11	BUS-55	11	BUS	GND			B
53	A1XA04-56	11	BUS-53	11	BUS	GND			B
318	A1XAC4-72	11	BUS-318	11	BUS	+15VDC			B
511*	A1XA05-C1	6	A1XAC3-2C	6	30SCL BK	TTXLOGND	TW2-511		
8	A1XA05-C2	11	BUS-8	11	BUS	+5VDC			
532	A1XAC5-C6	6	A1XA17-34	6	30SCL W	TXSYNRT			
511*	A1XA05-C7	6	A1XAC3-21	6	30SCL W	TTXLO	TW2-511		
524	A1XA05-C8	6	A1XA17-15	6	30SCL W	TXSYNRC			

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1C7C A 80063 SA-A-759628 F

SHEET 15

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
613*	A1XA05-11	6	A1XAC1-46	6	30SCL W	TXMX1			
526	A1XA05-11	6	A1XA14-11	6	30SCL W	TXMX1			
611*	A1XA05-12	6	A1XAC1-24	6	30SCL W	TXMX4			
528	A1XA05-12	6	A1XA14-12	6	30SOL W	TXMX4			
612*	A1XA05-14	6	A1XA01-60	6	30SCL W	TXMX2			
527	A1XAC5-14	6	A1XA14-14	6	30SCL W	TXMX2			
610*	A1XA05-15	6	A1XAC1-59	6	30SOL W	TXMX8			
529	A1XAC5-15	6	A1XA14-15	6	30SCL W	TXMX8			
525	A1XA05-16	6	A2XAC6-53	6	30SOL W	TBS2RC			
51	A1XA05-17	11	BUS-51	11	BUS	GND			B
52	A1XA05-18	11	BUS-52	11	BUS	GND			B
55	A1XA05-19	11	BUS-55	11	BUS	GND			B
53	A1XAC5-20	11	BUS-53	11	BUS	GND			B
1009	A1XA05-23	6	A1XAC6-22	6	30SOL W	TDUMP			B
576*	A1XA05-27	6	A1XAC2-39	6	30SCL W	T10100KT			
520	A1XA05-27	6	A1XA14-27	6	30SCL W	T10100KT			
512*	A1XA05-28	6	A1XAC3-14	6	30SOL W	TM1XD	TW2-512		
512*	A1XA05-29	6	A1XAC3-15	6	30SCL BK	TM1XDGND	TW2-512		
578*	A1XA05-30	6	A1XAC2-41	6	30SCL W	T100K1MT			
521	A1XA05-30	6	A1XA14-30	6	30SCL W	T100K1MT			
580*	A1XA05-31	6	A1XAC2-42	6	30SCL W	T1-10MT			
522	A1XA05-31	6	A1XA14-31	6	30SCL W	T1-10MT			
318	A1XAC5-36	11	BUS-318	11	BUS	+15VDC			B
8	A1XA05-38	11	BUS-8	11	BUS	+5VDC			
51	A1XAC5-53	11	BUS-51	11	BUS	GND			B
52	A1XA05-54	11	BUS-52	11	BUS	GND			B
55	A1XA05-55	11	BUS-55	11	BUS	GND			B
53	A1XA05-56	11	BUS-53	11	BUS	GND			B
318	A1XA05-72	11	BUS-318	11	BUS	+15VDC			B
8	A1XA06-02	11	BUS-8	11	BUS	+5VDC			
51	A1XA06-17	11	BUS-51	11	BUS	GND			B
52	A1XA06-18	11	BUS-52	11	BUS	GND			B
55	A1XA06-19	11	BUS-55	11	BUS	GND			B
53	A1XA06-20	11	BUS-53	11	BUS	GND			B
581*	A1XAC6-21	6	A1XAC2-35	6	30SCL W	TSAMP			
534	A1XAC6-21	6	A1XAC6-23	6	30SCL W	TSAMP			
1009*	A1XAC6-22	6	A1XAC5-23	6	30SOL W	TDUMP			B
534*	A1XAC6-23	6	A1XAC6-21	6	30SCL W	TSAMP			
299*	A1XA06-25	6	A1JC1-28	6	30SCL W	TSYNTST			
536*	A1XA06-29	14	ADAPTER 536	14	188 SHLD	GND		COAX	

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1070 A 80063 SM-A-759628 F

SHEET 16

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
536*	A1XA06-3C	14	ADAPTER	536 14 188	CTR	T45MVCO	COAX		
536*	A1XA06-31	14	ADAPTER	536 14 188	SHLD	GND	COAX		
75	A1XAC6-34	11	BUS-75	11	BUS	-15VDC			
318	A1XA06-36	11	BUS-318	11	BUS	+15VDC			
8	A1XA06-38	11	BUS-8	11	BUS	+5VDC			
51	A1XAC6-53	11	BUS-51	11	BUS	GND			B
52	A1XA06-54	11	BUS-52	11	BUS	GND			B
55	A1XA06-55	11	BUS-55	11	BUS	GND			B
53	A1XAC6-56	11	BUS-53	11	BUS	GND			B
536*	A1XA06-65	14	ADAPTER	536 14 188	SHLD	GND	COAX		
536*	A1XAC6-66	14	ADAPTER	536 14 188	CTR	T45MVCO	COAX		
536*	A1XA06-67	14	ADAPTER	536 14 188	SHLD	GND	COAX		
75	A1XA06-70	11	BUS-75	11	BUS	-15VDC			
318	A1XA06-72	11	BUS-318	11	BUS	+15VDC			
51	A1XA07-17	11	BUS-51	11	BUS	GND			B
52	A1XA07-18	11	BUS-52	11	BUS	GND			B
55	A1XA07-19	11	BUS-55	11	BUS	GND			B
53	A1XA07-20	11	BUS-53	11	BUS	GND			B
75	A1XA07-34	11	BUS-75	11	BUS	-15VDC			B
318	A1XAC7-36	11	BUS-318	11	BUS	+15VDC			B
51	A1XA07-53	11	BUS-51	11	BUS	GND			B
52	A1XAC7-54	11	BUS-52	11	BUS	GND			B
55	A1XA07-55	11	BUS-55	11	BUS	GND			B
53	A1XAC7-56	11	BUS-53	11	BUS	GND			B
75	A1XAC7-7C	11	BUS-75	11	BUS	-15VDC			B
318	A1XAC7-72	11	BUS-318	11	BUS	+15VDC			B
543*	A1XAC8-C9	14	ADAPTER	543 14 188	SHLD	GND	COAX		
543*	A1XAC8-1C	14	ADAPTER	543 14 188	CTR	TSCTCXO	COAX		
543*	A1XA08-11	14	ADAPTER	543 14 188	SHLD	GND	COAX		
545*	A1XAC8-12	14	ADAPTER	545 14 188	SHLD	GND	COAX		
545*	A1XA08-13	14	ADAPTER	545 14 188	CTR	T45MA	COAX		
545*	A1XA08-14	14	ADAPTER	545 14 188	SHLD	GND	COAX		
51	A1XAC8-17	11	BUS-51	11	BUS	GND			B
52	A1XA08-18	11	BUS-52	11	BUS	GND			B
55	A1XAC8-19	11	BUS-55	11	BUS	GND			B
53	A1XAC8-2C	11	BUS-53	11	BUS	GND			B
544*	A1XA08-21	14	ADAPTER	544 14 188	SHLD	GND	COAX		
544*	A1XAC8-22	14	ADAPTER	544 14 188	CTR	T45M1X	COAX		
544*	A1XA08-23	14	ADAPTER	544 14 188	SHLD	GND	COAX		
536*	A1XAC8-29	14	ADAPTER	536 14 188	SHLD	GND	COAX		

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1C7C A 80063 SM-A-759528 F

SHEET 17

WIRE NO.	FROM END	TERM	ENC	TO TERM		COLOR ITEM	REF NCDE	NOTE	REMARKS	REV
536*	A1XAC8-3C	14	ACAPTER	536	14	188 CTR	T45MVCO	COAX		
536*	A1XA08-31	14	ACAPTER	536	14	188 SHLD	GND	COAX		
75	A1XAC8-34	11	BUS-75		11	BUS	-15VDC			
318	A1XAC8-36	11	BUS-318		11	BUS	+15VDC			
543*	A1XA08-45	14	ACAPTER	543	14	188 SHLD	GND	COAX		
543*	A1XAC8-46	14	ACAPTER	543	14	188 CTR	TSCTCXO	COAX		
543*	A1XA08-47	14	ACAPTER	543	14	188 SHLD	GND	COAX		
545*	A1XAC8-4P	14	ACAPTER	545	14	188 SHLD	GND	COAX		
545*	A1XA08-49	14	ACAPTER	545	14	188 CTR	T45MA	COAX		
545*	A1XA08-50	14	ACAPTER	545	14	188 SHLD	GND	COAX		
51	A1XAC8-53	11	BUS-51		11	BUS	GND			B
52	A1XAC8-54	11	BUS-52		11	BUS	GND			B
55	A1XAC8-55	11	BUS-55		11	BUS	GND			B
53	A1XA08-56	11	BUS-53		11	BUS	GND			B
544*	A1XAC8-57	14	ACAPTER	544	14	188 SHLD	GND	COAX		
544*	A1XAC8-5E	14	ACAPTER	544	14	188 CTR	T45M1X	COAX		
544*	A1XAC8-59	14	ACAPTER	544	14	188 SHLD	GND	COAX		
536*	A1XAC8-65	14	ACAPTER	536	14	188 SHLD	GND	COAX		
536*	A1XAC8-66	14	ACAPTER	536	14	188 CTR	T45MVCO	COAX		
536*	A1XAC8-67	14	ACAPTER	536	14	188 SHLD	GND	COAX		
75	A1XAC8-70	11	BUS-75		11	BUS	-15VDC			
318	A1XAC8-72	11	BUS-318		11	BUS	+15VDC			
51	A1XA09-17	11	BUS-51		11	BUS	GND			B
52	A1XAC9-18	11	BUS-52		11	BUS	GND			B
55	A1XAC9-19	11	BUS-55		11	BUS	GND			B
53	A1XA09-20	11	BUS-53		11	BUS	GND			B
75	A1XA09-34	11	BUS-75		11	BUS	-15VDC			B
318	A1XA09-36	11	BUS-318		11	BUS	+15VDC			B
51	A1XA09-53	11	BUS-51		11	BUS	GND			B
52	A1XA09-54	11	BUS-52		11	BUS	GND			B
55	A1XA09-55	11	BUS-55		11	BUS	GND			B
53	A1XAC9-56	11	BUS-53		11	BUS	GND			B
75	A1XA09-7C	11	BUS-75		11	BUS	-15VDC			B
318	A1XAC9-72	11	BUS-318		11	BUS	+15VDC			B
510*	A1XA10-C2	14	ACAPTER	510	14	188 SHLD	GND	COAX		
510*	A1XA10-C3	14	ACAPTER	510	14	188 CTR	TM1XO	COAX		
510*	A1XA10-C4	14	ACAPTER	510	14	188 SHLD	GND	COAX		
551*	A1XA10-C5	14	ACAPTER	551	14	188 SHLD	GND	COAX		
551*	A1XA10-C6	14	ACAPTER	551	14	188 CTR	R15M1X	COAX		
551*	A1XA10-C7	14	ACAPTER	551	14	188 SHLD	GND	COAX		

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
544*	A1XA10-C8	14	ADAPTER	544 14 188	SHLD	GND	COAX		
544*	A1XA10-C9	14	ADAPTER	544 14 188	CTR	T45M1X	COAX		
544*	A1XA10-10	14	ADAPTER	544 14 188	SHLD	GND	COAX		
51	A1XA10-17	11	BUS-51	11	BUS	GND			B
52	A1XA10-18	11	BUS-52	11	BUS	GND			B
55	A1XA10-19	11	BUS-55	11	BUS	GND			B
53	A1XA10-20	11	BUS-53	11	BUS	GND			B
75	A1XA10-34	11	BUS-75	11	BUS	-15VDC			
318	A1XA10-36	11	BUS-318	11	BUS	+15VDC			
510*	A1XA10-38	14	ADAPTER	510 14 188	SHLD	GND	COAX		
510*	A1XA10-39	14	ADAPTER	510 14 188	CTR	TM1X0	COAX		
510*	A1XA10-4C	14	ADAPTER	510 14 188	SHLD	GND	COAX		
551*	A1XA10-41	14	ADAPTER	551 14 188	SHLD	GND	COAX		
551*	A1XA10-42	14	ADAPTER	551 14 188	CTR	R15M1X	COAX		
551*	A1XA10-43	14	ADAPTER	551 14 188	SHLD	GND	COAX		
544*	A1XA10-44	14	ADAPTER	544 14 188	SHLD	GND	COAX		
544*	A1XA10-45	14	ADAPTER	544 14 188	CTR	T45M1X	COAX		
544*	A1XA10-46	14	ADAPTER	544 14 188	SHLD	GND	COAX		
51	A1XA10-53	11	BUS-51	11	BUS	GND			B
52	A1XA10-54	11	BUS-52	11	BUS	GND			B
55	A1XA10-55	11	BUS-55	11	BUS	GND			B
53	A1XA10-56	11	BUS-53	11	BUS	GND			B
75	A1XA10-70	11	BUS-75	11	BUS	-15VDC			
318	A1XA10-72	11	BUS-318	11	BUS	+15VDC			
551*	A1XA11-15	14	ADAPTER	551 14 188	SHLD	GND	COAX		
551*	A1XA11-16	14	ADAPTER	551 14 188	CTR	R15M1X	COAX		
551*	A1XA11-17	14	ADAPTER	551 14 188	SHLD	GND	COAX		
51	A1XA11-17	11	BUS-51	11	BUS	GND			B
52	A1XA11-18	11	BUS-52	11	BUS	GND			B
55	A1XA11-19	11	BUS-55	11	BUS	GND			B
162*	A1XA11-2C	14	ADAPTER	162 14 188	SHLD	GND	COAX		
53	A1XA11-20	11	BUS-53	11	BUS	GND			B
162*	A1XA11-21	14	ADAPTER	162 14 188	CTR	TVCCNT	COAX		
162*	A1XA11-22	14	ADAPTER	162 14 188	SHLD	GND	COAX		
501	A1XA11-26	6	A1XA15-20	6	3CSCL EK	TBSBGND	TW2-501		
501	A1XA11-27	6	A1XA15-28	6	3CSCL W	TBSBSSC	TW2-501		
161*	A1XA11-29	14	ADAPTER	161 14 188	SHLD	GND	COAX		
161*	A1XA11-3C	14	ADAPTER	161 14 188	CTR	TVCC	COAX		
161*	A1XA11-31	14	ADAPTER	161 14 188	SHLD	GND	COAX		
75	A1XA11-34	11	BUS-75	11	BUS	-15VDC			

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 107C A 80C63 SM-A-759628 F

SHEET 19

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
318	A1XA11-36	11 BUS-318		11 BUS		+15VDC			
551*	A1XA11-51	14 ADAPTER	551	14 188	SHLD	GND	COAX		
551*	A1XA11-52	14 ADAPTER	551	14 188	CTR	R15M1X	COAX		
551*	A1XA11-53	14 ADAPTER	551	14 188	SHLD	GND	COAX		
51	A1XA11-53	11 BUS-51		11 BUS		GND			B
52	A1XA11-54	11 BUS-52		11 BUS		GND			B
55	A1XA11-55	11 BUS-55		11 BUS		GND			B
162*	A1XA11-56	14 ADAPTER	162	14 188	SHLD	GND	COAX		
53	A1XA11-56	11 BUS-53		11 BUS		GND			B
162*	A1XA11-57	14 ADAPTER	162	14 188	CTR	TVCONT	COAX		
162*	A1XA11-58	14 ADAPTER	162	14 188	SHLD	GND	COAX		
161*	A1XA11-65	14 ADAPTER	161	14 188	SHLD	GND	COAX		
161*	A1XA11-66	14 ADAPTER	161	14 188	CTR	TVCO	COAX		
161*	A1XA11-67	14 ADAPTER	161	14 188	SHLD	GND	COAX		
75	A1XA11-70	11 BUS-75		11 BUS		-15VDC			
318	A1XA11-72	11 BUS-318		11 BUS		+15VDC			
34	A1XA12-02	11 BUS-34		11 BUS		+5VDC			B
83	A1XA12-04	11 BUS-83		11 BUS		-5VDC			B
564	A1XA12-06	6 A1XA14-28		6 30SCL M		TSCMO			
543*	A1XA12-10	14 ADAPTER	543	14 188	SHLD	GND	COAX		
543*	A1XA12-11	14 ADAPTER	543	14 188	CTR	TSCTCXO	COAX		
543*	A1XA12-12	14 ADAPTER	543	14 188	SHLD	GND	COAX		
51	A1XA12-17	11 BUS-51		11 BUS		GND			B
52	A1XA12-18	11 BUS-52		11 BUS		GND			B
55	A1XA12-19	11 BUS-55		11 BUS		GND			B
53	A1XA12-20	11 BUS-53		11 BUS		GND			B
509*	A1XA12-27	14 ADAPTER	509	14 188	SHLD	GND	COAX		
509*	A1XA12-28	14 ADAPTER	509	14 188	CTR	TSC45M	COAX		
509*	A1XA12-29	14 ADAPTER	509	14 188	SHLD	GND	COAX		
75	A1XA12-34	11 BUS-75		11 BUS		-15VDC			B
318	A1XA12-36	11 BUS-318		11 BUS		+15VDC			B
34	A1XA12-38	11 BUS-34		11 BUS		+5VDC			B
83	A1XA12-40	11 BUS-83		11 BUS		-5VDC			B
543*	A1XA12-46	14 ADAPTER	543	14 188	SHLD	GND	COAX		
543*	A1XA12-47	14 ADAPTER	543	14 188	CTR	TSCTCXO	COAX		
543*	A1XA12-48	14 ADAPTER	543	14 188	SHLD	GND	COAX		
51	A1XA12-53	11 BUS-51		11 BUS		GND			B
52	A1XA12-54	11 BUS-52		11 BUS		GND			B
55	A1XA12-55	11 BUS-55		11 BUS		GND			B
53	A1XA12-56	11 BUS-53		11 BUS		GND			B

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1C7C A 8C063 SM-A-759528 F

SHEET 20

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
509*	A1XA12-63	14	ADAPTER	509 14	188 SHLD	GND	COAX		
509*	A1XA12-64	14	ADAPTER	509 14	188 CTR	TSC45M	COAX		
509*	A1XA12-65	14	ADAPTER	509 14	188 SHLD	GND	COAX		
75	A1XA12-70	11	BUS-75	11	BUS	-15VDC			B
318	A1XA12-72	11	BUS-318	11	BUS	+15VDC			B
34	A1XA13-C2	11	BUS-34	11	BUS	+5VDC			B
75	A1XA13-34	11	BUS-75	11	BUS	-15VDC			B
318	A1XA13-36	11	BUS-318	11	BUS	+15VDC			B
34	A1XA13-38	11	BUS-34	11	BUS	+5VDC			B
75	A1XA13-3C	11	BUS-75	11	BUS	-15VDC			B
318	A1XA13-72	11	BUS-318	11	BUS	+15VDC			B
963	A1XA14-C1	6	A1XA14-C7	6	30SOL BK	DSTBCK			B
57	A1XA14-C1	11	BUS-57	11	BUS	GND			B
34	A1XA14-02	11	BUS-34	11	BUS	+5VDC			
963*	A1XA14-C7	6	A1XA14-01	6	30SOL BK	DSTBCK			B
566	A1XA14-C8	6	A1XA21-16	6	30SOL W	TXSYNTR			
526*	A1XA14-11	6	A1XAC5-11	6	30SOL W	TXMX1			
528*	A1XA14-12	6	A1XAC5-12	6	30SOL W	TXMX4			
527*	A1XA14-14	6	A1XAC5-14	6	30SOL W	TXMX2			
529*	A1XA14-15	6	A1XAC5-15	6	30SOL W	TXMX8			
520*	A1XA14-27	6	A1XAC5-27	6	30SOL W	T100100KT			
564*	A1XA14-28	6	A1XA12-C8	6	30SOL W	TSCMO			
521*	A1XA14-3C	6	A1XAC5-3C	6	30SOL W	T100K1MT			
522*	A1XA14-31	6	A1XAC5-31	6	30SOL W	T1-10MT			
75	A1XA14-34	11	BUS-75	11	BUS	-15VDC			B
318	A1XA14-36	11	BUS-318	11	BUS	+15VDC			B
57	A1XA14-37	11	BUS-57	11	BUS	GND			B
34	A1XA14-38	11	BUS-34	11	BUS	+5VDC			
75	A1XA14-70	11	BUS-75	11	BUS	-15VDC			B
318	A1XA14-72	11	BUS-318	11	BUS	+15VDC			B
57	A1XA15-C1	11	BUS-57	11	BUS	GND			B
34	A1XA15-C2	11	BUS-34	11	BUS	+5VDC			
486	A1XA15-C6	6	A1XA16-C8	6	30SOL W	TDAC-1			
482	A1XA15-C7	6	A1XA16-20	6	30SOL W	TDAC-2			
483	A1XA15-C8	6	A1XA16-07	6	30SOL W	TDAC-3			
484	A1XA15-C5	6	A1XA16-11	6	30SOL W	TDAC-4			
485	A1XA15-1C	6	A1XA16-14	6	30SOL W	TDAC-5			
481	A1XA15-11	6	A1XA16-30	6	30SOL W	TDAC-6			
479	A1XA15-12	6	A1XA16-C8	6	30SOL W	TDAC-8			
480	A1XA15-13	6	A1XA16-33	6	30SOL W	TDAC-7			

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
495	A1XA15-15	6	A1XA16-31	6	30SCL W	CACCLK			
501*	A1XA15-2C	6	A1XA11-26	6	30SCL BK	TBSBGND	TW2-501		
501*	A1XA15-28	6	A1XA11-27	6	30SCL W	TBSBSSC	TW2-501		
75	A1XA15-34	11	BUS-75	11	BUS	-15VDC			
318	A1XA15-36	11	BUS-318	11	BUS	+15VDC			
57	A1XA15-37	11	BUS-57	11	BUS	GND			B
34	A1XA15-38	11	BUS-34	11	BUS	+5VDC			
75	A1XA15-70	11	BUS-75	11	BUS	-15VDC			B
318	A1XA15-72	11	BUS-318	11	BUS	+15VDC			
57	A1XA16-C1	11	BUS-57	11	BUS	GND			
34	A1XA16-C2	11	BUS-34	11	BUS	+5VDC			
483*	A1XA16-C7	6	A1XA15-C8	6	30SCL W	TCAC-3			
486*	A1XA16-CE	6	A1XA15-C6	6	30SCL W	TCAC-1			
484*	A1XA16-11	6	A1XA15-C9	6	30SCL W	TCAC-4			
485*	A1XA16-14	6	A1XA15-10	6	30SCL W	TCAC-5			
471	A1XA16-15	6	A1XA16-16	6	30SCL W	LFMSBT			
471*	A1XA16-16	6	A1XA16-15	6	30SCL W	LFMSBT			
470	A1XA16-16	6	A1XA16-17	6	30SCL W	LFMSBT			
470*	A1XA16-17	6	A1XA16-16	6	30SCL W	LFMSBT			
469	A1XA16-17	6	A1XA17-23	6	30SCL W	LFMSBT			
468	A1XA16-18	6	A1XA17-24	6	30SCL W	LFTRANT			
482*	A1XA16-20	6	A1XA15-C7	6	30SCL W	TCAC-2			
472	A1XA16-24	6	A1XA17-36	6	30SCL W	LPFCLKT			
481*	A1XA16-2C	6	A1XA15-11	6	30SCL W	TCAC-6			
495*	A1XA16-31	6	A1XA15-15	6	30SCL W	CACCLK			
467	A1XA16-31	6	A1XA17-35	6	30SCL W	CACCLK			
480*	A1XA16-33	6	A1XA15-13	6	30SCL W	TCAC-7			
57	A1XA16-37	11	BUS-57	11	BUS	GND			
34	A1XA16-38	11	BUS-34	11	BUS	+5VDC			
477	A1XA16-66	6	A1XA17-14	6	30SCL W	LFUNDRT			
479*	A1XA16-68	6	A1XA15-12	6	30SCL W	TCAC-8			
478	A1XA16-69	6	A1XA17-25	6	30SCL W	LFCVERC			
57	A1XA17-C1	11	BUS-57	11	BUS	GND			
34	A1XA17-C2	11	BUS-34	11	BUS	+5VDC			
228	A1XA17-C8	6	A2XAC7-23	6	30SCL W	TBSDATT			
90	A1XA17-C9	6	A2XAC6-42	6	30SCL W	TBSDATC			
687	A1XA17-12	6	A2XAC4-26	6	30SCL W	TXBSDTT			
477*	A1XA17-14	6	A1XA16-66	6	30SCL W	LFUNDRT			
524*	A1XA17-15	6	A1XAC5-C8	6	30SCL W	TXSYNRC			
452	A1XA17-19	6	A2XAC6-C9	6	30SCL W	TXSYNRC			

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1C7C A 80C63 SM-A-759628 F

SHEET 22

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
466	A1XA17-17	6	A2XA10-2E	6	30SCL W	TBSLOLC			
469*	A1XA17-23	6	A1XA1E-17	6	30SCL W	LFMSBT			
468*	A1XA17-24	6	A1XA1E-18	6	30SCL W	LFTRANT			
478*	A1XA17-25	6	A1XA1E-E9	6	30SCL W	LFOVERC			
532*	A1XA17-34	6	A1XAC5-C6	6	30SCL W	TXSYNRT			
451	A1XA17-34	6	A2XAC4-24	6	30SCL W	TXSYNRT			
467*	A1XA17-35	6	A1XA1E-31	6	30SCL W	CACCLK			
460	A1XA17-35	6	A2XAC7-15	6	30SCL W	CACCLK			
472*	A1XA17-36	6	A1XA1E-24	6	30SCL W	LPFCLKT			
57	A1XA17-37	11	BUS-57	11	BUS	GND			
34	A1XA17-38	11	BUS-34	11	BUS	+5VDC			
1C49	A1XA21-C2	11	BUS-1C49	11	BUS	+5VDC			B
106	A1XA21-C4	11	BUS-1C6	11	BUS	-5VDC			
566*	A1XA21-16	6	A1XA14-C8	6	30SCL W	TXSYNTR			
81	A1XA21-17	11	BUS-81	11	BUS	GND			B
86	A1XA21-18	11	BUS-E6	11	BUS	GND			B
89	A1XA21-19	11	BUS-E9	11	BUS	GND			B
385	A1XA21-2C	6	A1XA21-21$	9	26SCL BK	GND		SHLD PGT-384, INTCLKS	
82	A1XA21-20	11	BUS-E2	11	BUS	GND			B
384	A1XA21-21	6	A2J02-15	6	26SCL W	INTCLK+		STW2-384	B
385*	A1XA21-21$	9	A1XA21-20	6	26SCL BK	GND		SHLD PGT-384, INTCLKS	
384	A1XA21-21$	9	A2J02-15$	9	ERAID SH	GND		STW2-384	
384	A1XA21-22	6	A2J02-16	6	26SCL BK	INTCLK-		STW2-384	B
386	A1XA21-23	6	A2XAC7-41	6	30SCL W	INTCLKT			
1C55	A1XA21-25	6	A2XAC3-C7	6	30SCL W	TXDATA			F
1C56	A1XA21-31	6	A2XAC2-32	6	30SCL W	NRZDR+			F
1057	A1XA21-32	6	A2XAC2-30	6	30SCL W	NRZDR-			F
1C49	A1XA21-38	11	BUS-1C49	11	BUS	+5VDC			B
106	A1XA21-4C	11	BUS-1C6	11	BUS	-5VDC			
81	A1XA21-53	11	BUS-81	11	BUS	GND			B
86	A1XA21-54	11	BUS-E6	11	BUS	GND			B
89	A1XA21-55	11	BUS-E9	11	BUS	GND			B
82	A1XA21-56	11	BUS-E2	11	BUS	GND			B
1049	A1XA22-C2	11	BUS-1C49	11	BUS	+5VDC			B
106	A1XA22-C4	11	BUS-1C6	11	BUS	-5VDC			
378	A1XA22-16	6	A1XA22-16	6	30SCL W	DATOUT			
81	A1XA22-17	11	BUS-81	11	BUS	GND			B
86	A1XA22-18	11	BUS-E6	11	BUS	GND			B
89	A1XA22-19	11	BUS-E9	11	BUS	GND			B
816	A1XA22-20	7	A1XA22-22$	9	26SCL BK	GND		SHLD PGT-315	B

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SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1C7C A 8CC63 SM-A-759628 F

SHEET 23

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
82	A1XA22-20	11	BUS-E2	11	BLS	GND			B
815	A1XA22-21	6	A2J02-04	6	26SCL BK	ALTCOUT-		STW2-815	B
815	A1XA22-22	6	A2J02-03	6	26SCL W	ALTOUT+		STW2-815	B
816*	A1XA22-22$	9	A1XA22-20	7	26SCL BK	GND		SHLD PGT-815	B
815	A1XA22-22$	9	A2J02-03$	9	BRAID SH	GND		STW2-815	
230	A1XA22-23	6	A2XAC7-19	6	30SCL W	ALTOUTT			
234	A1XA22-25	6	A1XA23-25	6	30SCL W	CLKOUTT			
233	A1XA22-26	6	A2XAC7-32	6	30SCL W	ALTCLKT			
820	A1XA22-30	6	A1XA22-31$	9	26SCL BK	GND		SHLD PGT-374	B
374	A1XA22-31	6	A2J02-33	6	26SCL W	ALTCLK+		STW2-374	
820*	A1XA22-31$	9	A1XA22-30	6	26SCL BK	GND		SHLD PGT-374	B
374	A1XA22-31$	9	A2J02-33$	9	BRAID SH	GND		STW2-374	
374	A1XA22-32	6	A2J02-34	6	26SCL BK	ALTCLK-		STW2-374	
1049	A1XA22-38	11	BUS-1049	11	BUS	+5VDC			B
106	A1XA22-40	11	BUS-106	11	BUS	-5VDC			
81	A1XA22-53	11	BUS-E1	11	BUS	GND			B
86	A1XA22-54	11	BUS-E6	11	BUS	GND			B
89	A1XA22-55	11	BUS-89	11	BUS	GND			B
82	A1XA22-56	11	BUS-E2	11	BUS	GND			B
1049	A1XA23-C2	11	BUS-1049	11	BUS	+5VDC			B
106	A1XA23-C4	11	BUS-106	11	BUS	-5VDC			
378*	A1XA23-16	6	A1XA22-16	6	30SCL W	CATOUTT			
364	A1XA23-16	6	A2XAC6-66	6	30SCL W	CATOUTT			
81	A1XA23-17	11	BUS-E1	11	BUS	GND			B
86	A1XA23-18	11	BUS-E6	11	BUS	GND			B
89	A1XA23-19	11	BUS-89	11	BUS	GND			B
836	A1XA23-20	7	A1XA22-22$	9	26SCL BK	GND		SHLD PGT-835	B
82	A1XA23-2C	11	BUS-E2	11	BUS	GND			B
835	A1XA23-21	6	A2J02-06	6	26SCL BK	CATOUT-		STW2-835	B
835	A1XA23-22	6	A2J02-05	6	26SCL W	CATOUT+		STW2-835	B
836*	A1XA23-22$	9	A1XA23-20	7	26SCL BK	GND		SHLD PGT-835	B
835	A1XA23-22$	9	A2J02-05$	9	BRAID SH	GND		STW2-835	
226	A1XA23-23	6	A2XAC7-24	6	30SCL W	BUFCUTT			
234*	A1XA23-25	6	A1XA22-25	6	30SCL W	CLKCUTT			
365	A1XA23-25	6	A2XAC6-58	6	30SCL W	CLKCUTT			
367	A1XA23-26	6	A2XAC7-35	6	30SCL W	BCKCUTT			
840	A1XA23-30	6	A1XA23-31$	9	26SCL BK	GND		SHLD PGT-839	B
839	A1XA23-31	6	A2J02-13	6	26SCL W	CLKOUT+		STW2-339	B
840*	A1XA23-31$	9	A1XA23-30	6	26SCL BK	GND		SHLD PGT-839	B
839	A1XA23-31$	9	A2J02-13$	9	BRAID SH	GND		STW2-839	

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
839	A1XA23-32	6	A2JC2-14	6	26SOL BK	CLKOUT-	STW2-839		B
1049	A1XA23-38	11	BUS-1C49	11	BUS	+5VDC			B
106	A1XA23-4C	11	BUS-1C6	11	BUS	-5VDC			
81	A1XA23-53	11	BUS-E1	11	BUS	GND			B
86	A1XA23-54	11	BUS-E6	11	BUS	GND			B
89	A1XA23-55	11	BUS-E9	11	BUS	GND			B
82	A1XA23-56	11	BUS-E2	11	BUS	GND			B
68	A2J01-C1	7	A2J01-11	6	26SCL BK	GND			
11	A2J01-C1	7	W1-	12	E-24 BK	GND			
971	A2J01-C2	6	A2XAC1-24	6	30SCL R	+5VDC			B
1022	A2J01-C2	6	A2XAC2-C2	7	30SOL R	+5VDC	ICF		B
575*	A2J01-C3	6	A1XAC2-C3	6	30SCL W	T10-100K			
1011*	A2J01-C4	6	A1XAC2-C6	6	30SOL W	T1-10M			B
1010*	A2J01-C5	6	A1XAC2-C5	6	30SOL W	T100K-1M			B
6*	A2J01-C6	6	A1XAC1-14	6	30SCL W	TO-COM			
7*	A2J01-C7	6	A1XAC1-65	6	30SCL W	TX9-0-1			
639*	A2J01-C8	6	A1XAC1-25	6	30SCL W	TX9-0-2			
9*	A2J01-C9	6	A1XAC1-27	6	30SCL W	TX9-0-4			
10*	A2J01-10	6	A1XAC1-66	6	30SCL W	TX9-0-8			
68*	A2J01-11	6	A2JC1-01	7	26SCL BK	GND			
293	A2J01-11	6	A2J03-01	6	26SCL BK	GND			
12*	A2J01-12	6	A1XAC1-15	6	30SOL W	T1-COM			
13*	A2J01-13	6	A1XA01-69	6	30SCL W	TX9-1-1			
14*	A2J01-14	6	A1XAC1-3C	6	30SCL W	TX9-1-2			
15*	A2J01-15	6	A1XAC1-63	6	30SCL W	TX9-1-4			
16*	A2J01-16	6	A1XAC1-68	6	30SCL W	TX9-1-8			
17*	A2J01-17	6	A1XAC1-23	6	30SCL W	T2-COM			
18*	A2J01-18	6	A1XA01-41	6	30SCL W	TX9-2-1			
19*	A2J01-19	6	A1XAC1-C8	6	30SCL W	TX9-2-2			
20*	A2J01-20	6	A1XAC1-44	6	30SCL W	TX9-2-4			
26*	A2J01-21	6	A1XAC1-42	6	30SCL W	TX9-2-8			
21*	A2J01-23	6	A1XAC1-51	6	30SCL W	T3-COM			
22*	A2J01-24	6	A1XAC1-C5	6	30SCL W	TX9-3-1			
23*	A2J01-25	6	A1XAC1-43	6	30SCL W	TX9-3-2			
24*	A2J01-26	6	A1XAC1-54	6	30SCL W	TX9-3-4			
25*	A2J01-27	6	A1XAC1-56	6	30SCL W	TX9-3-8			
27*	A2J01-33	6	A1XAC1-52	6	30SCL W	T4-COM			
28*	A2J01-34	6	A1XAC1-58	6	30SCL W	TX9-4-1			
29*	A2J01-35	6	A1XAC1-47	6	30SCL W	TX9-4-2			
30*	A2J01-36	6	A1XAC1-10	6	30SCL W	TX9-4-4			

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HIGHEST WIRE NUMBER IS 1C7C A 80063 SM-A-759628 F

SHEET 25

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
31*	A2J01-37	6	A1XAC1-22	6	30SCL W	TX9-4-8			
63	A2J02-C1	6	A2J02-03$	9	26SCL BK	GND		SHLD PGT 815	
289	A2J02-01	6	A2JC3-01	6	26SCL BK	GND			
815*	A2J02-C3	6	A1XA22-22	6	26SCL W	ALTOUT+		STW2-815	B
815*	A2J02-C3$	9	A1XA22-22$	9	BRAID SH	GND		STW2-815	
63*	A2J02-C3$	9	A2JC2-C1	6	26SCL BK	GND		SHLD PGT 815	
815*	A2JC2-C4	6	A1XA22-21	6	26SCL BK	ALTOUT-		STW2-815	B
835*	A2J02-C5	6	A1XA23-22	6	26SCL W	CATOUT+		STW2-835	B
835*	A2JC2-C5$	9	A1XA23-22$	9	BRAID SH	GND		STW2-835	
64	A2J02-05$	9	A2J02-11	6	26SCL BK	GND		SHLD PGT 835	
835*	A2J02-C6	6	A1XA23-21	6	26SCL BK	CATOUT-		STW2-835	B
1034	A2J02-C7	6	A2XAC1-C5	6	30SCL W	ICFIN75+		TW2-1034	B
1034	A2J02-C8	6	A2XAC1-10	6	30SCL BK	ICFIN75-		TW2-1034	B
64*	A2J02-11	6	A2JC2-C5$	9	26SCL BK	GND		SHLD PGT 835	
117	A2J02-11	6	A2JC2-13$	9	26SCL BK	GND		SHLD PGT 839	
118	A2J02-12	6	A2JC2-15$	9	26SCL BK	GND		SHLD PGT 384	
69	A2J02-12	6	A2JC2-17$	9	26SCL BK	GND		SHLD PGT 672	
839*	A2J02-13	6	A1XA23-31	6	26SCL W	CLKOUT+		STW2-839	B
839*	A2J02-13$	9	A1XA23-31$	9	BRAID SH	GND		STW2-839	
117*	A2J02-13$	9	A2J02-11	6	26SCL BK	GND		SHLD PGT 839	
839*	A2J02-14	6	A1XA23-32	6	26SCL BK	CLKOUT-		STW2-839	B
384*	A2J02-15	6	A1XA21-21	6	26SCL W	INTCLK+		STW2-384	B
384*	A2JC2-15$	9	A1XA21-21$	9	BRAID SH	GND		STW2-384	
118*	A2J02-15$	9	A2JC2-12	6	26SCL BK	GND		SHLD PGT 384	
384*	A2J02-16	6	A1XA21-22	6	26SCL BK	INTCLK-		STW2-384	B
672	A2JC2-17	6	A2XAC4-33	6	26SCL W	INCLK+		STW2-672	
69*	A2J02-17$	9	A2J02-12	6	26SCL BK	GND		SHLD PGT 672	
672	A2J02-17$	9	A2XAC4-33$	9	BRAID SH	GND		STW2-672	
672	A2J02-18	6	A2XAC4-32	6	26SCL BK	INCLK-		STW2-672	
1059	A2J02-19	6	A2XAC2-29	6	30SCL W	BALIN+		TW2-1059	F
1059	A2J02-20	6	A2XAC2-28	6	30SCL BK	BALIN-		TW2-1059	F
960	A2J02-23	6	A2XAC3-31	6	30SCL W	ICFCU50+		TW2-960	B
960	A2J02-24	6	A2XAC3-30	6	30SCL BK	ICFCU50-		TW2-960	B
1036	A2J02-25	6	A2XAC1-C6	6	30SCL W	ICFIN50+		TW2-1036	B
1036	A2J02-26	6	A2XAC1-C7	6	30SCL BK	ICFIN50-		TW2-1036	B
P4	A2J02-27	6	A2XA1C-40	6	30SCL W	EXTALM2			
1004	A2J02-28	6	A2XA1C-39	6	30SCL W	EXTAL41		ICF	B
959	A2J02-29	6	A2XAC3-29	6	30SCL W	CLCST		TW2-959	B
959	A2J02-30	6	A2XAC3-30	6	30SCL BK	CLCSG		TW2-959	B
72	A2J02-31	6	A2JC2-33$	9	26SCL BK	GND		SHLD PGT 374	

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
79	A2J02-32	6	A2J02-39$	9	26SOL BK	GND		SHLD PGT 670	
374*	A2J02-33	6	A1XA22-31	6	26SOL W	ALTCLK+		STW2-374	
374*	A2J02-33$	9	A1XA22-31$	9	BRAID SH	GND		STW2-374	
72*	A2J02-33$	9	A2J02-31	6	26SOL BK	GND		SHLD PGT 374	
374*	A2J02-34	6	A1XA22-32	6	26SOL BK	ALTCLK-		STW2-374	
961	A2J02-35	6	A2XAC3-22	6	30SOL W	ICFCU75+		TW2-961	B
961	A2J02-36	6	A2XAC3-24	6	30SOL BK	ICFCU75-		TW2-961	B
1058	A2J02-37	6	A2XAC2-26	6	30SOL W	EALOUT+		TW2-1058	F
1058	A2J02-38	6	A2XAC2-25	6	30SOL BK	EALOUT-		TW2-1058	F
670	A2J02-39	6	A2XAC4-30	6	26SOL W	INSTD+		STW2-670	
79*	A2J02-39$	9	A2J02-32	6	26SOL BK	GND		SHLD PGT 670	
670	A2J02-39$	8	A2XAC4-30$	8	BRAID SH	GND		STW2-670	
670	A2J02-40	6	A2XAC4-28	6	26SOL BK	INSTD-		STW2-670	
293*	A2J03-01	6	A2J01-11	6	26SOL BK	GND			
289*	A2J03-01	6	A2J02-01	6	26SOL BK	GND			
712	A2J03-05	6	A2XAC5-22	6	30SOL W	SGNTD+		TW2-712	B
712	A2J03-06	6	A2XAC5-23	6	30SOL BK	SGNTD-		TW2-712	B
751	A2J03-07	6	A2XAC5-68	6	30SOL W	2RCKFE+		TW2-751	B
751	A2J03-08	6	A2XAC5-69	6	30SOL BK	2RCKFE-		TW2-751	B
724	A2J03-13	6	A2XAC5-58	6	30SOL W	RCKFD+		TW2-724	B
724	A2J03-14	6	A2XAC5-59	6	30SOL BK	RCKFD-		TW2-724	B
710	A2J03-15	6	A2XAC5-48	6	30SOL W	2RCKTE+		TW2-710	B
710	A2J03-16	6	A2XAC5-49	6	30SOL BK	2RCKTE-		TW2-710	B
723	A2J03-17	6	A2XAC5-33	6	30SOL W	DATFE+		TW2-723	B
723	A2J03-18	6	A2XAC5-34	6	30SOL BK	DATFE-		TW2-723	B
725	A2J03-23	6	A2XAC5-61	6	30SOL W	DATFD+		TW2-725	B
725	A2J03-24	6	A2XAC5-60	6	30SOL BK	DATFD-		TW2-725	B
709	A2J03-25	6	A2XAC5-56	6	30SOL W	RCKTE+		TW2-709	B
709	A2J03-26	6	A2XAC5-57	6	30SOL BK	RCKTE-		TW2-709	B
987	A2J03-27	6	A2XAC5-11	6	30SOL W	MSBTD+		TW2-987	B
987	A2J03-28	6	A2XAC5-12	6	30SOL BK	MSBTD-		TW2-987	B
736	A2J03-33	6	A2XAC5-44	6	30SOL W	RCKTD+		TW2-736	B
736	A2J03-34	6	A2XAC5-45	6	30SOL BK	RCKTD-		TW2-736	B
737	A2J03-35	6	A2XAC5-46	6	30SOL W	2RCKTD+		TW2-737	B
737	A2J03-36	6	A2XAC5-47	6	30SOL BK	2RCKTD-		TW2-737	B
711	A2J03-37	6	A2XAC5-24	6	30SOL W	DATTE+		TW2-711	B
711	A2J03-38	6	A2XAC5-25	6	30SOL BK	DATTE-		TW2-711	B
1037*	A2XAC1-C1	15	ADAPTER 1037	15	188 SHLD	GND		COAX	B
1037*	A2XA01-C2	15	ADAPTER 1037	15	188 CTR	LOSINB+		COAX	B
1037*	A2XA01-C3	15	ADAPTER 1037	15	188 SHLD	GND		COAX	B

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1070 A 80063 SM-A-759628 F

SHEET 27

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
1C36*	A2XA01-C6	6	A2J02-25	6	30SCL W	ICFIN50+	TW2-1036		B
1036*	A2XA01-C7	6	A2J02-26	6	30SCL BK	ICFIN50-	TW2-1036		B
1034*	A2XA01-C9	6	A2J02-C7	6	30SCL W	ICFIN75+	TW2-1034		B
1034*	A2XA01-1C	6	A2J02-08	6	30SCL BK	ICFIN75-	TW2-1034		B
1060	A2XA01-12	6	A2XAC2-C8	6	30SCL W	NRZREC+			F
1C61	A2XA01-15	6	A2XAC2-09	6	30SCL W	NRZREC-			F
97	A2XA01-17	11	BUS-97	11	BUS	GND			B
95	A2XA01-18	11	BUS-95	11	BUS	GND			B
93	A2XA01-19	11	BUS-93	11	BUS	GND			B
1C18	A2XA01-2C	11	BUS-1C18	11	BUS	GND			B
1C33	A2XA01-22	6	A2XAC3-32	6	30SCL W	TSTICF			B
571*	A2XA01-24	6	A2J01-02	6	30SCL R	+5VDC			B
570	A2XA01-24	6	A2XAC2-C2	7	30SCL R	+5VDC			B
565*	A2XA01-25	6	A1J01-17	6	30SCL W	ICFRLYE			B
1062	A2XA01-25	6	A2XAC2-11	6	30SCL W	ICFRLY			F
1032	A2XA01-27	6	A2XAC4-C8		30SCL W	ICF2			B
1C23	A2XA01-33	6	A2XAC4-C7	6	30SCL W	ICF1			B
76	A2XA01-34	11	BUS-76	11	BUS	-15VDC			
316	A2XA01-3E	11	BUS-316	11	BUS	+15VDC			
1037*	A2XA01-37	15	ADAPTER 1037	15	188 SHLD	GND	COAX		B
1037*	A2XA01-3E	15	ADAPTER 1037	15	188 CTR	LCSINB+	COAX		B
1037*	A2XA01-39	15	ADAPTER 1037	15	188 SHLD	GND	COAX		B
97	A2XA01-53	11	BUS-97	11	BUS	GND			B
95	A2XA01-54	11	BUS-95	11	BUS	GND			B
93	A2XA01-55	11	BUS-93	11	BUS	GND			B
1018	A2XA01-5E	11	BUS-1018	11	BUS	GND			B
76	A2XA01-70	11	BUS-76	11	BUS	-15VDC			
316	A2XAC1-72	11	BUS-316	11	BUS	+15VDC			
1C69	A2XA02-C1	6	A2XAC2-17	6	30SCL BK	GND			F
1022*	A2XA02-C2	7	A2JC1-C2	6	30SCL R	+5VDC	ICF		B
570*	A2XAC2-C2	7	A2XAC1-24	6	30SCL R	+5VDC			B
35	A2XA02-02	11	BUS-35	11	BUS	+5VDC			
1C67	A2XA02-C4	6	A2XAC4-40	6	30SCL G	-5VDC			F
1C60*	A2XA02-C8	6	A2XAC1-12	6	30SCL W	NRZREC+			F
1C61*	A2XA02-C9	6	A2XAC1-15	6	30SCL W	NRZREC-			F
1C63	A2XAC2-1C	6	A2XAC4-10	6	30SCL W	NRZDATA			F
1C62*	A2XA02-11	6	A2XAC1-25	6	30SCL W	ICFRLY			F
1C65	A2XA02-12	6	A2XAC7-11	6	30SCL W	PNSEQ			F
1C66	A2XA02-13	6	A2XAC7-63	6	30SCL W	TEST3			F
1C69*	A2XA02-17	6	A2XAC2-C1	6	30SCL BK	GND			F

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1C7C A 80063 SM-A-759628 F

SHEET 28

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
97	A2XA02-17	11	BUS-97	11	BLS	GND			E
1070	A2XA02-18	6	A2XA02-37	6	30SCL BK	GND			F
95	A2XA02-18	11	BUS-95	11	BLS	GND			B
93	A2XA02-19	11	BUS-93	11	BLS	GND			B
1018	A2XA02-20	11	BUS-1018	11	BLS	GND			B
1058*	A2XA02-25	6	A2JC2-38	6	30SCL BK	BALOUT-		TW2-1058	F
1058*	A2XA02-26	6	A2JC2-37	6	30SCL W	BALOUT+		TW2-1058	F
1064	A2XA02-27	6	A2XA11-12	6	30SCL W	RECDATA			F
1059*	A2XA02-28	6	A2JC2-20	6	30SCL BK	BALIN-		TW2-1059	F
1059*	A2XA02-29	6	A2JC2-19	6	30SCL W	BALIN+		TW2-1059	F
1057*	A2XA02-30	6	A1XA21-32	6	30SCL W	NRZDR-			F
1053	A2XA02-31	6	A2XAC3-16	6	30SOL W	ICFDR-			F
1056*	A2XA02-32	6	A1XA21-31	6	30SCL W	NRZDR+			F
1054	A2XA02-33	6	A2XAC3-21	6	30SCL W	ICFDR+			F
76	A2XA02-34	11	BUS-76	11	BLS	-15VDC			
316	A2XA02-36	11	BUS-316	11	BLS	+15VDC			
1070*	A2XA02-37	6	A2XA02-18	6	30SCL BK	GND			F
35	A2XA02-38	11	BUS-35	11	BUS	+5VDC			
1068	A2XA02-40	6	A2XAC4-40	6	30SCL G	-5VDC			F
97	A2XA02-53	11	BUS-97	11	BLS	GND			B
95	A2XA02-54	11	BUS-95	11	BLS	GND			B
93	A2XA02-55	11	BUS-93	11	BUS	GND			B
1018	A2XAC2-56	11	BUS-1018	11	BLS	GND			B
76	A2XA02-70	11	BUS-76	11	BUS	-15VDC			
316	A2XAC2-72	11	BUS-316	11	BLS	+15VDC			
35	A2XAC3-02	11	BUS-35	11	BUS	+5VDC			
952	A2XA03-06	6	A2XAC6-67	6	30SOL W	ICFCLKT			B
1055*	A2XA03-07	6	A1XA21-25	6	30SCL W	TXDATA			F
951	A2XA03-07	6	A2XAC6-25	6	30SCL W	ICFDATT			B
1053*	A2XAC3-16	6	A2XAC2-31	6	30SCL W	ICFDR-			F
97	A2XA03-17	11	BUS-97	11	BUS	GND			B
95	A2XA03-18	11	BUS-95	11	BUS	GND			B
93	A2XA03-19	11	BUS-93	11	BUS	GND			B
1018	A2XA03-20	11	BUS-1018	11	BUS	GND			B
1054*	A2XA03-21	6	A2XAC2-33	6	30SCL W	ICFDR+			F
961*	A2XA03-22	6	A2JC2-35	6	30SCL W	ICFCU75+		TW2-961	E
961*	A2XA03-24	6	A2JC2-36	6	30SOL BK	ICFCU75-		TW2-961	B
959*	A2XA03-25	6	A2JC2-25	6	30SCL W	OLOST		TW2-959	B
960*	A2XA03-30	6	A2JC2-24	6	30SCL BK	ICFCU50-		TW2-960	B
959*	A2XA03-30	6	A2JC2-30	6	30SCL BK	OLOSG		TW2-959	B

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1070 A 80063 SM-A-759628 F

SHEET 29

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
960*	A2XAC3-31	6	A2JC2-23	6	30SCL W	ICFOU50+	TW2-960		B
1033*	A2XAC3-32	6	A2XAC1-22	6	30SCL W	TSTICF			B
76	A2XAC3-34	11	BUS-76	11	BUS	-15VDC			
316	A2XAC3-36	11	BUS-316	11	BUS	+15VDC			
35	A2XAC3-38	11	BUS-35	11	BUS	+5VDC			
97	A2XAC3-53	11	BUS-97	11	BUS	GND			B
95	A2XAC3-54	11	BUS-95	11	BUS	GND			B
93	A2XAC3-55	11	BUS-93	11	BUS	GND			B
1018	A2XAC3-56	11	BUS-1018	11	BUS	GND			B
76	A2XAC3-70	11	BUS-76	11	BUS	-15VDC			
316	A2XAC3-72	11	BUS-316	11	BUS	+15VDC			
35	A2XAC4-C2	11	BUS-35	11	BUS	+5VDC			
972	A2XAC4-C3	6	A2XAC4-27	6	30SCL W	ENTXGT			B
706	A2XAC4-C4	11	BUS-706	11	BUS	-5VDC			
1023*	A2XAC4-C7	6	A2XAC1-33	6	30SCL W	ICF1			B
1032*	A2XAC4-C8		A2XAC1-27	6	30SCL W	ICF2			B
1063*	A2XAC4-10	6	A2XAC2-10	6	30SCL W	NRZDATA			F
681	A2XAC4-12	6	A2XAC7-59	6	30SCL W	TSEQ+			
279*	A2XAC4-13	6	A1J01-05	6	30SCL W	ENOPERC			
682	A2XAC4-13	6	A2XAC7-C6	6	30SCL W	ENOPERC			
281*	A2XAC4-14	6	A1J01-07	6	30SCL W	ENTESTC			
169*	A2XAC4-15	6	A1J02-05	6	30SCL W	ENCLKRC			
677	A2XAC4-15	6	A2XAC6-16	6	30SCL W	ENCLKRC			
676*	A2XAC4-16	6	A1J02-06	6	30SCL W	ENSTDRC			
97	A2XAC4-17	11	BUS-97	11	BUS	GND			B
95	A2XAC4-18	11	BUS-95	11	BUS	GND			B
93	A2XAC4-19	11	BUS-93	11	BUS	GND			B
1018	A2XAC4-2C	11	BUS-1018	11	BUS	GND			B
685	A2XAC4-22	6	A2XAC6-C6	6	30SCL W	CBSDATC			
451*	A2XAC4-24	6	A1XA17-34	6	30SCL W	TXSYNRT			
687*	A2XAC4-26	6	A1XA17-12	6	30SCL W	TXBSDTT			
972*	A2XAC4-27	6	A2XAC4-C3	6	30SCL W	ENTXGT			B
670*	A2XAC4-28	6	A2JC2-40	6	26SCL BK	INSTD-	STW2-670		
671	A2XAC4-29	6	A2XAC4-30$	8	26SCL BK	GND	SHLD PGT-670,INSTDS		
670*	A2XAC4-30	6	A2JC2-39	6	26SCL W	INSTD+	STW2-670		
670*	A2XAC4-3C$	8	A2JC2-39$	8	BRAID SH	GND	STW2-670		
671*	A2XAC4-3C$	8	A2XAC4-29	6	26SCL BK	GND	SHLD PGT-670,INSTDS		
673	A2XAC4-31	6	A2XAC4-33$	5	26SCL BK	GND	SHLD PGT-672,INCLKS		
672*	A2XAC4-32	6	A2JC2-18	6	26SCL BK	INCLK-	STW2-672		
672*	A2XAC4-33	6	A2JC2-17	6	26SCL W	INCLK+	STW2-672		

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1C7C A 80063 SM-A-759628 F

SHEET 30

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
672*	A2XA04-33$	9	A2J02-17$	5	BRAID SH	GND		STW2-672	
673*	A2XA04-33$	9	A2XAC4-31	6	26SOL BK	GND		SHLD PGT-672, INCLKS	
35	A2XA04-38	11	BUS-35	11	BLS	+5VDC			
1067*	A2XA04-4C	6	A2XAC2-C4	6	30SCL G	-5VDC			F
1C68*	A2XA04-40	6	A2XAC2-4C	6	30SCL G	-5VDC			F
7C6	A2XA04-40	11	BUS-7C6	11	BLS	-5VDC			
97	A2XA04-53	11	BLS-97	11	BUS	GND			B
95	A2XA04-54	11	BUS-95	11	BLS	GND			B
93	A2XA04-55	11	BLS-93	11	BUS	GND			B
1018	A2XA04-56	11	BLS-1C18	11	BLS	GND			B
975	A2XAC5 C8	6	A2XAC5-C7	6	30SCL BK	GND			B
104	A2XAC5-01	11	BLS-1C4	11	BUS	GND			
35	A2XA05-02	11	BUS-35	11	BLS	+5VDC			
718	A2XA05-C4	7	A2XAC9-48	6	30SCL G	-5VDC			
706	A2XAC5-C4	11	BLS-7C6	11	BLS	-5VDC			
974	A2XA05-C5	6	A2XAC5-C7	6	30SCL BK	GND			B
949	A2XAC5-C5	6	A2XA05-08	6	30SCL BK	GND			B
975*	A2XAC5-C7	6	A2XAC5 C8	6	30SCL BK	GND			B
974*	A2XAC5-C7	6	A2XA05-C5	6	30SCL BK	GND			B
950	A2XAC5-C7	6	A2XAC5-C8	6	30SCL BK	GND			B
949*	A2XA05-C8	6	A2XAC5-05	6	30SCL BK	GND			B
950*	A2XA05-C8	6	A2XAC5-C7	6	30SCL BK	GND			B
987*	A2XAC5-11	6	A2J03-27	6	30SCL W	MSBTD+		TW2-987	B
987*	A2XAC5-12	6	A2J03-28	6	30SCL BK	MSBTD-		TW2-987	B
713	A2XAC5-15	6	A2XAC6-51	6	30SCL W	CATTENT			
742	A2XA05-16	6	A2XAC6-32	6	30SOL W	RBSDATT			
712*	A2XA05-22	6	A2J03-05	6	30SOL W	SGNTD+		TW2-712	B
712*	A2XA05-23	6	A2J03-06	6	30SCL BK	SGNTD-		TW2-712	B
711*	A2XA05-24	6	A2J03-37	6	30SCL W	CATTE+		TW2-711	B
711*	A2XA05-25	6	A2J03-38	6	30SCL BK	CATTE-		TW2-711	B
1012	A2XAC5-26	6	A2XAC5-27	6	30SCL BK	GND			B
1013	A2XA05-26	6	A2XAC5-28	6	30SOL BK	GND			B
1012*	A2XAC5-27	6	A2XAC5-26	6	30SCL BK	GND			E
1013*	A2XA05-28	6	A2XAC5-26	6	30SCL BK	GND			B
723*	A2XAC5-33	6	A2J03-17	6	30SCL W	CATFE+		TW2-723	B
723*	A2XAC5-34	6	A2J03-18	6	30SCL BK	CATFE-		TW2-723	B
104	A2XA05-37	11	BLS-1C4	11	BLS	GND			
35	A2XAC5-38	11	BLS-35	11	BLS	+5VDC			
706	A2XA05-4C	11	BLS-7C6	11	BUS	-5VDC			
956	A2XAC5-41	6	A2XAC7-39	6	30SCL W	RBSERT			B

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1C7C A 80063 SM-A-759628 F

SHEET 31

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
576	A2XAC5-42	6	A2XAC7-C8	6	30SOL W	RCKTDCT			B
736*	A2XAC5-44	6	A2JC3-33	6	30SOL W	RCKTD+		TW2-736	B
736*	A2XAC5-45	6	A2JC3-34	6	30SOL BK	RCKTD-		TW2-736	B
737*	A2XAC5-46	6	A2JC3-35	6	30SOL W	2RCKTD+		TW2-737	B
737*	A2XAC5-47	6	A2JC3-36	6	30SOL BK	2RCKTD-		TW2-737	B
710*	A2XAC5-48	6	A2JC3-15	6	30SOL W	2RCKTE+		TW2-710	B
710*	A2XAC5-49	6	A2JC3-16	6	30SOL BK	2RCKTE-		TW2-710	B
585	A2XAC5-50	6	A2XAC7-31	6	30SOL W	B			B
740	A2XAC5-51	6	A2XAC6-47	6	30SOL W	RCLKTET			
709*	A2XAC5-56	6	A2JC3-25	6	30SOL W	RCKTE+		TW2-709	B
709*	A2XAC5-57	6	A2JC3-26	6	30SOL BK	RCKTE-		TW2-709	B
724*	A2XAC5-58	6	A2JC3-13	6	30SOL W	RCKFD+		TW2-724	B
724*	A2XAC5-59	6	A2JC3-14	6	30SOL BK	RCKFD-		TW2-724	B
725*	A2XAC5-6C	6	A2JC3-24	6	30SOL BK	DATFD-		TW2-725	B
725*	A2XAC5-61	6	A2JC3-23	6	30SOL W	DATFD+		TW2-725	B
746	A2XAC5-62	6	A2XAC6-13	6	30SOL W	EXTDECT			
750	A2XAC5-63	6	A2XAC6-69	6	30SOL W	DATFDCC			
749	A2XAC5-64	6	A2XAC6-64	6	30SOL W	RCKFDCT			
748	A2XAC5-65	6	A2XAC6-C7	6	30SOL W	DATFENC			
745	A2XAC5-66	6	A2XAC6-11	6	30SOL W	EXTENCT			
747	A2XAC5-67	6	A2XAC6-46	6	30SOL W	2RCKFEC			
751*	A2XAC5-68	6	A2JC3-07	6	30SOL W	2RCKFE+		TW2-751	B
751*	A2XAC5-69	6	A2JC3-08	6	30SOL BK	2RCKFE-		TW2-751	B
104	A2XAC6-C1	11	BUS-104	11	BUS	GND			
35	A2XAC6-C2	11	BUS-35	11	BUS	+5VDC			
685*	A2XAC6-C6	6	A2XAC4-22	6	30SOL W	CBSDATC			
748*	A2XAC6-C7	6	A2XAC5-65	6	30SOL W	DATFENC			
452*	A2XAC6-C9	6	A1XA17-15	6	30SOL W	TXSYNRC			
94	A2XAC6-C9	6	A2XAC6-43	6	30SOL W	TXSYNRC			
278*	A2XAC6-1C	6	A1JC1-04	6	30SOL W	EXTENCC			
745*	A2XAC6-11	6	A2XAC5-66	6	30SOL W	EXTENCT			
746*	A2XAC6-13	6	A2XAC5-62	6	30SOL W	EXTDECT			
167*	A2XAC6-14	6	A1JC2-03	6	30SOL W	DIFDECT			
277*	A2XAC6-15	6	A1JC1-C3	6	30SOL W	NCENCC			
677*	A2XAC6-16	6	A2XAC4-15	6	30SOL W	ENCLKRC			
166*	A2XAC6-22	6	A1JC2-02	6	30SOL W	DIFENCC			
951*	A2XAC6-25	6	A2XAC3-C7	6	30SOL W	ICFDATT			B
99	A2XAC6-26	6	A2XAC6-27	6	30SOL W	DISABL			
578	A2XAC6-26	6	A2XAC6-29	6	30SOL W	DISABL			B
99*	A2XAC6-27	6	A2XAC6-26	6	30SOL W	DISABL			

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
103	A2XA06-27	6	A2XAC6-28	6	30SCL W	DISABL			
103*	A2XA06-28	6	A2XAC6-27	6	30SCL W	DISABL			
98	A2XA06-28	6	A2XAC6-54	6	30SCL W	DISABL			
978*	A2XA06-29	6	A2XAC6-26	6	30SCL W	DISABL			B
1024	A2XAC6-29	6	A2XAC6-54	6	30SCL W	DISABL			B
1025	A2XAC6-29	6	A2XA06-68	6	30SCL W	DISABL			B
742*	A2XA06-32	6	A2XAC5-16	6	30SCL W	RBSDATT			
100	A2XA06-32	6	A2XAC7-58	6	30SCL W	RBSCATT			
165	A2XAC6-33	6	A2XAC7-56	6	30SCL W	RBSBRC			
104	A2XA06-37	11	BUS-104	11	BUS	GND			
35	A2XA06-38	11	BUS-35	11	BUS	+5VDC			
90*	A2XA06-42	6	A1XA17-09	6	30SCL W	TBSDATC			
94*	A2XAC6-43	6	A2XAC6-09	6	30SCL W	TXSYNRC			
953	A2XAC6-44	6	A2XAC6-45	6	30SCL W	DISABL			B
953*	A2XA06-45	6	A2XAC6-44	6	30SCL W	DISABL			B
954	A2XA06-45	6	A2XAC6-54	6	30SCL W	DISABL			B
747*	A2XA06-46	6	A2XAC5-67	6	30SCL W	2RCKFEC			
740*	A2XA06-47	6	A2XAC5-51	6	30SCL W	RCLKTET			
284*	A2XA06-48	6	A1JC1-1C	6	30SCL W	EXTDECC			
713*	A2XA06-51	6	A2XAC5-15	6	30SCL W	CATTENT			
96	A2XA06-52	6	A2XAC6-53	6	30SCL W	TBS2RC			
525*	A2XA06-53	6	A1XAC5-16	6	30SCL W	TBS2RC			
96*	A2XA06-53	6	A2XAC6-52	6	30SCL W	TBS2RC			
98*	A2XA06-54	6	A2XAC6-28	6	30SCL W	DISABL			
1024*	A2XA06-54	6	A2XAC6-29	6	30SCL W	DISABL			B
954*	A2XA06-54	6	A2XAC6-45	6	30SCL W	DISABL			B
983	A2XA06-55	6	A2XAC7-67	6	30SCL W	AA			B
365*	A2XAC6-58	6	A1XA23-25	6	30SCL W	CLKOUTT			
283*	A2XA06-59	6	A1JC1-09	6	30SCL W	NODECC			
749*	A2XAC6-64	6	A2XAC5-64	6	30SCL W	FCKFDCT			
364*	A2XA06-66	6	A1XA23-16	6	30SCL W	DATOUTT			
952*	A2XA06-67	6	A2XAC3-06	6	30SCL W	ICFCLKT			B
1025*	A2XAC6-68	6	A2XAC6-29	6	30SCL W	DISABL			B
750*	A2XA06-69	6	A2XAC5-63	6	30SCL W	CATFDCC			
980	A2XAC7-01	7	A2XAC7-53	6	30SCL BK	GND			B
104	A2XAC7-01	11	BUS-104	11	BUS	GND			
35	A2XAC7-02	11	BUS-35	11	BUS	+5VDC			
148	A2XAC7-05	6	A2XAC7-45	6	30SCL W	SOGENCK			
682*	A2XAC7-06	6	A2XAC4-13	6	30SCL W	ENCPERC			
976*	A2XAC7-0F	6	A2XAC5-42	6	30SCL W	RCKTDCT			B

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
558	A2XAC7-C5	6	A2XAC7-10	6	30SCL W	A			B
958*	A2XAC7-1C	6	A2XAC7-C9	6	30SCL W	A			B
1065*	A2XAC7-11	6	A2XAC7-12	6	30SCL W	ENSEQ			F
227	A2XA07-11	6	A2XAC7-59	6	30SOL W	TSEQ+			
405*	A2XA07-13	6	A1J01-33	6	30SCL W	SYNCN11	TW2-405		
150	A2XAC7-14	6	A2XAC7-66	6	30SCL W	SGN-11			
460*	A2XAC7-15	6	A1XA17-35	6	30SCL W	DACCLK			
130	A2XA07-16	6	A2XAC7-55	6	30SCL W	CLKOUTC			
213	A2XAC7-17	6	A2XAC8-25	6	30SCL W	CCMPCKT			
230*	A2XAC7-19	6	A1XA22-23	6	30SCL W	ALTOUTT			
228*	A2XA07-22	6	A1XA17-C8	6	30SCL W	TBSDATT			
226*	A2XAC7-24	6	A1XA23-23	6	30SCL W	BUFOUTT			
215	A2XAC7-25	6	A2XAC8-32	6	30SCL W	CCMPDTC			
138*	A2XA07-27	6	A1JC1-11	6	30SCL W	TSTSEQ			
585*	A2XA07-31	6	A2XAC5-50	6	30SCL W	B			B
233*	A2XAC7-32	6	A1XA22-26	6	30SCL W	ALTCLKT			
217	A2XAC7-33	6	A2XA07-57	6	30SCL W	ALTCLKC			
367*	A2XAC7-35	6	A1XA23-26	6	30SCL W	BCKOUTT			
405*	A2XAC7-37	6	A1J01-34	6	30SCL BK	SYNCGND	TW2-405		
406*	A2XAC7-37	6	A1JC1-36	6	30SCL BK	CCMPGND	TW2-406		
104	A2XA07-37	11	BUS-1C4	11	BUS	GND			
35	A2XAC7-38	11	BUS-35	11	BUS	+5VDC			
556*	A2XA07-39	6	A2XAC5-41	6	30SCL W	RBSBRT			B
386*	A2XAC7-41	6	A1XA21-23	6	30SCL W	INTCLKT			
555	A2XAC7-42	6	A2XA11-36	6	30SCL W	RBSBRT			B
211	A2XAC7-43	6	A2XAC7-51	6	30SCL W	TSEQBRC			
148*	A2XA07-45	6	A2XAC7-C5	6	30SCL W	SQGENCK			
225	A2XAC7-5C	6	A2XAC7-56	6	30SCL W	RBSBRC			
211*	A2XAC7-51	6	A2XAC7-43	6	30SCL W	TSEQBRC			
406*	A2XAC7-52	6	A1J01-35	6	30SCL W	CCMPCKC	TW2-406		
580*	A2XAC7-53	6	A2XAC7-01	7	30SCL BK	GND			B
579	A2XA07-53	6	A2XAC7-61	6	30SOL BK	GND			B
130*	A2XAC7-55	6	A2XAC7-1E	6	30SCL W	CLKOUTC			
224	A2XA07-55	6	A2XAC7-71	6	30SCL W	CLKOUTC			
165*	A2XAC7-56	6	A2XAC6-33	6	30SCL W	RBSBRC			
225*	A2XAC7-56	6	A2XAC7-50	6	30SCL W	RBSBRC			
846	A2XA07-56	6	A2XA13-15	6	30SOL W	RBSBRC			
217*	A2XA07-57	6	A2XAC7-33	6	30SCL W	ALTCLKC			
100*	A2XA07-58	6	A2XAC6-32	6	30SCL W	RBSDATT			
1028	A2XA07-58	6	A2XA11-C8	6	30SCL W	RBSDATT			B

(SYNTH & 31T SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 107C A 8C063 SM-A-759628 F

SHEET 34

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
681*A2XAC7-59		6	A2XAC4-12	6	30SCL W	TSEQ+			
227*A2XAC7-59		6	A2XAC7-11	6	30SCL W	TSEQ+			B
579*A2XAC7-61		6	A2XAC7-53	6	30SCL BK	GND			
139*A2XA07-62		6	A1J01-12	6	30SOL W	TSTTX8S			
287*A2XAC7-63		6	A1J01-13	6	30SCL W	TSTRX8S			
1066*A2XA07-63		6	A2XAC2-13	6	30SCL W	TEST3			F
141*A2XA07-65		6	A1J01-15	6	30SCL W	TSTALT			
150*A2XA07-66		6	A2XAC7-14	6	30SCL W	SGN-11			
583*A2XAC7-67		6	A2XAC6-55	6	30SCL W	AA			B
584 A2XA07-68		6	A2XAC7-69	6	30SCL W	AAA			B
584*A2XA07-69		6	A2XAC7-68	6	30SCL W	AAA			B
274*A2XA07-71		6	A2XAC7-55	6	30SCL W	CLKOUTC			
300 A2XAC8-C1		7	A2XAC6-21	6	30SCL BK	GND			
104 A2XAC8-C1		11	BUS-104	11	BUS	GND			
35 A2XAC8-C2		11	BUS-35	11	BUS	+5VDC			
269 A2XA08-03		6	A2XAC5-44	6	30SCL W	BRD256C			
265 A2XAC8-C6		6	A2XAC8-68	6	30SCL W	CTN-11			
260 A2XAC8-12		6	A2XAC6-13	6	30SCL W	PULLUP+			
260*A2XA08-13		6	A2XAC6-12	6	30SCL W	PULLUP+			
257 A2XA08-13		6	A2XAC6-19	6	30SCL W	PULLUP+			
271 A2XAC8-14		6	A2XAC8-36	6	30SCL W	SMFSTRC			
257*A2XAC8-19		6	A2XAC8-13	6	30SCL W	PULLUP+			
262 A2XAC8-19		6	A2XAC6-20	6	30SCL W	PULLUP+			
262*A2XAC8-20		6	A2XAC6-19	6	30SCL W	PULLUP+			
261 A2XAC8-20		6	A2XAC6-29	6	30SCL W	PULLUP+			
300*A2XAC8-21		6	A2XAC8-01	7	30SCL BK	GND			
272 A2XA08-21		6	A2XAC6-22	6	30SOL BK	GND			
272*A2XAC8-22		6	A2XAC6-21	6	30SCL BK	GND			
273 A2XAC8-22		6	A2XAC6-28	6	30SCL BK	GND			
266 A2XAC8-23		6	A2XAC6-24	6	30SCL W	CCMPCVC			
266*A2XAC8-24		6	A2XAC8-23	6	30SCL W	CCMPCVC			
253 A2XA08-24		6	A2XAC5-C7	6	30SOL W	CCMPCVC			
213*A2XAC8-25		6	A2XAC7-17	6	30SCL W	CCMPCKT			
251 A2XA08-25		6	A2XAC5-10	6	30SOL W	CCMPCKT			
274*A2XAC8-28		6	A1J01-32	6	30SCL BK	ERRGND		TW2-274	
273*A2XAC8-28		6	A2XAC6-22	6	30SCL BK	GND			
261*A2XA08-29		6	A2XAC6-20	6	30SCL W	PULLUP+			
263 A2XAC8-29		6	A2XAC6-43	6	30SCL W	PULLUP+			
291*A2XA08-30		6	A1J01-19	6	30SCL W	ERRCNT			
215*A2XAC8-32		6	A2XAC7-25	6	30SCL W	COMPDTC			

(SYNTH & BIT SYNC)

SIZE	CODE IDENT NO.		REV
A	80063	SM-A-759628	F

HIGHEST WIRE NUMBER IS 1070

SHEET 35

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
250	A2XAC8-32	6	A2XAC9-46	6	30SCL W	CCMPDTC			
274*	A2XAC8-33	6	A1JC1-31	6	30SCL W	ERRCUT	TW2-274		
271*	A2XAC8-36	6	A2XAC8-14	6	30SCL W	SMPSTRC			
104	A2XAC8-37	11	BUS-104	11	BUS	GND			
35	A2XAC8-38	11	BUS-35	11	BUS	+5VDC			
263*	A2XAC8-43	6	A2XAC8-25	6	30SCL W	PULLUP+			
258	A2XAC8-43	6	A2XAC8-47	6	30SCL W	PULLUP+			
258*	A2XAC8-47	6	A2XAC8-43	6	30SCL W	PULLUP+			
254*	A2XAC8-50	6	A1JC1-30	6	30SCL W	CMPATDC			
303	A2XAC8-51	6	A2XAC9-45	6	30SCL W	CMPERRT			
402*	A2XAC8-52	6	A1JC1-29	6	30SCL W	MANSMPC			
265*	A2XAC8-68	6	A2XAC8-06	6	30SCL W	CTN-11			
104	A2XAC9-01	11	BUS-104	11	BUS	GND			
35	A2XAC9-02	11	BUS-35	11	BUS	+5VDC			
253*	A2XAC9-07	6	A2XAC8-24	6	30SCL W	CCMPCVC			
1CC8*	A2XAC9-08	6	A1JC1-26	6	30SCL W	ERRSIG	TW2-1CC8		B
1C08*	A2XAC9-09	6	A1JC1-27	6	30SCL BK	ERRGND	TW2-1008		B
251*	A2XAC9-10	6	A2XAC8-25	6	30SCL W	COMPCKT			
306	A2XAC9-10	6	A2XAC9-12	6	30SCL W	COMPCKT			
294*	A2XAC9-11	6	A1JC1-22	6	30SCL W	TESTP5V			
306*	A2XAC9-12	6	A2XAC9-10	6	30SCL W	CCMPCKT			
319	A2XAC9-13	6	A2XAC9-36	7	30SCL O	+15VDC			B
1051	A2XAC9-13	6	A2XA3-36	6	30SCL O	+15VDC			
187*	A2XAC9-14	6	A1JC2-35	6	30SCL W	CATZER			
581	A2XAC9-15	6	A2XAC9-43	6	30SCL V	-15VDC			B
582	A2XAC9-15	6	A2XA12-34	7	30SCL V	-15VDC			B
297*	A2XAC9-16	6	A1JC1-25	6	30SCL W	TESTM15			
319*	A2XAC9-36	7	A2XAC9-13	6	30SCL O	+15VDC			B
104	A2XAC9-37	11	BUS-104	11	BUS	GND			
313	A2XAC9-38	7	A2XAC9-47	6	30SCL R	+5VDC			
35	A2XAC9-38	11	BUS-35	11	BUS	+5VDC			
581*	A2XAC9-43	6	A2XAC9-15	6	30SCL V	-15VDC			B
269*	A2XAC9-44	6	A2XAC8-03	6	30SCL W	ERD256C			
303*	A2XAC9-45	6	A2XAC8-51	6	30SCL W	CMPERRT			
250*	A2XAC9-46	6	A2XAC8-32	6	30SCL W	CCMPDTC			
313*	A2XAC9-47	6	A2XAC9-38	7	30SCL R	+5VDC			
718*	A2XAC9-48	6	A2XAC5-04	7	30SCL G	-5VDC			
255*	A2XAC9-49	6	A1JC1-23	6	30SCL W	TESTM5V			
188*	A2XAC9-50	6	A1JC2-37	6	30SCL W	CATCNE			
312*	A2XAC9-51	6	A1JC2-31	6	30SCL W	CLKZER			

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1C7C A 80063 SM-A-759628 F

SHEET 36

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
296*	A2XA09-52	6	A1JC1-24	6	30SCL W	TESTP15			
314*	A2XA09-57	6	A1JC2-33	6	30SCL W	CLKONE			
104	A2XA10-01	11	BUS-1C4	11	BUS	GND			
35	A2XA10-02	11	BUS-35	11	BUS	+5VDC			
566*	A2XA10-03	6	A1JC2-27	6	30SCL W	TXFAIL			B
181*	A2XA10-09	6	A1JC2-23	6	30SCL W	TXBSFL			
178*	A2XA10-12	6	A1JC2-17	6	30SCL W	RXBSLOL			
180*	A2XA10-22	6	A1JC2-21	6	30SCL W	RXFAIL			
466*	A2XA10-28	6	A1XA17-17	6	30SCL W	TBSLOLC			
990	A2XA10-31	6	A2XA11-17	6	30SCL W	LOSSLTC			B
596	A2XA10-32	6	A2XA1C-35	6	30SCL W	CSALMG			B
596*	A2XA10-35	6	A2XA10-32	6	30SCL W	CSALMG			B
1031	A2XA10-35	6	A2XA1C-63	6	30SCL W	CSALMG			B
104	A2XA10-37	11	BUS-1C4	11	BUS	GND			
35	A2XA10-38	11	BUS-35	11	BUS	+5VDC			
1004*	A2XA10-39	6	A2JC2-28	6	30SOL W	EXTALM1	ICF		B
84*	A2XA10-40	6	A2JC2-27	6	30SCL W	EXTALM2			
1029*	A2XA10-45	6	A1JC2-C7	6	30SCL W	AUDALM1			B
175*	A2XA10-46	6	A1JC2-11	6	30SCL W	THERMO			
766*	A2XA10-47	6	A1JC2-C8	6	30SCL W	AUDALM2			
756*	A2XA10-52	6	A1JC2-10	6	30SCL W	ALMRST			
1031*	A2XA10-63	6	A2XA1C-35	6	30SCL W	CSALMG			B
597	A2XA10-66	6	A2XA10-68	6	30SCL W	CSALMG			B
597*	A2XA10-68	6	A2XA1C-66	6	30SCL W	CSALMG			B
104	A2XA11-01	11	BUS-1C4	11	BUS	GND			B
35	A2XA11-02	11	BUS-35	11	BUS	+5VDC			B
1028*	A2XA11-08	6	A2XAC7-58	6	30SCL W	RBSDATT			B
1064*	A2XA11-12	6	A2XAC2-27	6	30SCL W	RECDATA			F
588	A2XA11-14	6	A2XA12-66	6	30SCL W	RLFUNDT			B
1026	A2XA11-15	6	A2XA2C-C8	6	30SCL W	RXSYNRC	TW2-1026		B
590*	A2XA11-17	6	A2XA10-31	6	30SCL W	LOSSLTC			B
591	A2XA11-23	6	A2XA12-17	6	30SOL W	RSIGNT			B
592	A2XA11-24	6	A2XA12-1F	6	30SCL W	RTRANT			B
593	A2XA11-25	6	A2XA12-69	6	30SOL W	RLFCURC			B
1027	A2XA11-34	6	A2XA2C-C6	6	30SCL W	RXSYNRT	TW2-1027		B
594	A2XA11-35	6	A2XA12-31	6	30SCL W	RBSBRC			B
595*	A2XA11-36	6	A2XAC7-42	6	30SCL W	RBSBRT			B
595	A2XA11-36	6	A2XA12-24	6	30SCL W	RBSBRT			B
1026	A2XA11-37	7	A2XA2C-37	7	30SCL BK	GND	TW2-1026		B
1027	A2XA11-37	7	A2XA2C-37	7	30SCL BK	GND	TW2-1027		B

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
104	A2XA11-37	11	BUS-1C4	11	BUS	GND			B
35	A2XA11-38	11	BUS-35	11	BUS	+5VDC			B
104	A2XA12-C1	11	BUS-1C4	11	BUS	GND			B
35	A2XA12-C2	11	BUS-35	11	BUS	+5VDC			B
889	A2XA12-C7	6	A2XA13-C8	6	30SOL W	RDAC-3			
892	A2XA12-CE	6	A2XA13-C6	6	30SCL W	RDAC-1			
890	A2XA12-11	6	A2XA13-09	6	30SCL W	RDAC-4			
891	A2XA12-14	6	A2XA13-10	6	30SOL W	RDAC-5			
1017	A2XA12-15	6	A2XA12-16	6	30SCL W	RSIGNT			B
1017*	A2XA12-16	6	A2XA12-15	6	30SOL W	RSIGNT			B
1016	A2XA12-1E	6	A2XA12-17	6	30SCL W	RSIGNT			B
591*	A2XA12-17	6	A2XA11-23	6	30SCL W	RSIGNT			B
1016*	A2XA12-17	6	A2XA12-16	6	30SCL W	RSIGNT			B
592*	A2XA12-18	6	A2XA11-24	6	30SCL W	RTRANT			B
888	A2XA12-2C	6	A2XA13-C7	6	30SCL W	RDAC-2			
595*	A2XA12-24	6	A2XA11-36	6	30SCL W	RBSBRT			B
887	A2XA12-30	6	A2XA13-11	6	30SCL W	RDAC-6			
994*	A2XA12-31	6	A2XA11-35	6	30SCL W	RBSBRC			B
882	A2XA12-31	6	A2XA13-15	6	30SCL W	RBSBRC			
886	A2XA12-33	6	A2XA13-13	6	30SCL W	RDAC-7			
582*	A2XA12-34	7	A2XAC9-15	6	30SCL W	-15VDC			B
864	A2XA12-34	11	BUS-E64	11	BUS	-15VDC			
104	A2XA12-37	11	BUS-1C4	11	BUS	GND			B
35	A2XA12-3E	11	BUS-35	11	BUS	+5VDC			B
588*	A2XA12-66	6	A2XA11-14	6	30SCL W	RLFUNDT			B
881	A2XA12-68	6	A2XA13-12	6	30SCL W	RDAC-8			
593*	A2XA12-69	6	A2XA11-25	6	30SCL W	RLFOURC			B
864	A2XA12-70	11	BUS-E64	11	BUS	-15VDC			
35	A2XA13-C2	11	BUS-35	11	BUS	+5VDC			B
892*	A2XA13-CE	6	A2XA12-CE	6	30SCL W	RDAC-1			
888*	A2XA13-C7	6	A2XA12-2C	6	30SCL W	RDAC-2			
889*	A2XA13-C8	6	A2XA12-C7	6	30SCL W	RDAC-3			
890*	A2XA13-C9	6	A2XA12-11	6	30SCL W	RDAC-4			
891*	A2XA13-1C	6	A2XA12-14	6	30SCL W	RDAC-5			
887*	A2XA13-11	6	A2XA12-30	6	30SOL W	RDAC-6			
881*	A2XA13-12	6	A2XA12-68	6	30SCL W	RDAC-8			
886*	A2XA13-13	6	A2XA12-33	6	30SCL W	RDAC-7			
846*	A2XA13-15	6	A2XAC7-56	6	30SOL W	RBSBRC			
882*	A2XA13-15	6	A2XA12-31	6	30SCL W	RBSBRC			
853	A2XA13-17	11	GND BUS-B53	11	BUS	GND			

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1C7C A 80063 SM-A-759628 F

SHEET 38

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
E54	A2XA13-18	11	GND BUS-E54	11	BUS	GND			
E55	A2XA13-19	11	GND BUS-E55	11	BUS	GND			
883	A2XA13-20	6	A2XA14-28	6	30SCL BK	RTN		TW2-893	
E56	A2XA13-20	11	GND BUS-E56	11	BUS	GND			
E64	A2XA13-34	11	BUS-E64	11	BUS	-15VDC			
E48	A2XA13-36	11	BUS-E48	11	BUS	+15VDC			
35	A2XA13-38	11	BUS-35	11	BUS	+5VDC			B
E53	A2XA13-53	11	GND BUS-E53	11	BUS	GND			
E54	A2XA13-54	11	GND BUS-E54	11	BUS	GND			
E55	A2XA13-55	11	GND BUS-E55	11	BUS	GND			
E56	A2XA13-56	11	GND BUS-E56	11	BUS	GND			
E83	A2XA13-64	6	A2XA14-27	6	30SCL W	RBSBSSC		TW2-883	
E64	A2XA13-70	11	BUS-E64	11	BUS	-15VDC			
E48	A2XA13-72	11	BUS-E48	11	BUS	+15VDC			
947*	A2XA14-15	14	ADAPTER 947	14	183 SHLD	GND		COAX	
947*	A2XA14-16	14	ADAPTER 947	14	189 CTR	R15M1X		COAX	
947*	A2XA14-17	14	ADAPTER 947	14	188 SHLD	GND		COAX	
E53	A2XA14-17	11	GND BUS-E53	11	BUS	GND			
E54	A2XA14-18	11	GND BUS-E54	11	BUS	GND			
E55	A2XA14-19	11	GND BUS-E55	11	BUS	GND			
861*	A2XA14-20	15	ADAPTER E61	15	188 SHLD	GND		COAX	
856	A2XA14-20	11	GND BUS-E56	11	BUS	GND			
861*	A2XA14-21	15	ADAPTER E61	15	189 CTR	RVCCNT		COAX	
861*	A2XA14-22	15	ADAPTER 861	15	183 SHLD	GND		COAX	
E83*	A2XA14-27	6	A2XA13-64	6	30SCL W	RBSBSSC		TW2-883	
883*	A2XA14-28	6	A2XA13-20	6	30SCL BK	RTN		TW2-893	
860*	A2XA14-29	15	ADAPTER 860	15	188 SHLD	GND		COAX	
860*	A2XA14-30	15	ADAPTER 86C	15	188 CTR	RVCC		COAX	
860*	A2XA14-31	15	ADAPTER 860	15	188 SHLD	GND		COAX	
E64	A2XA14-34	11	BUS-E64	11	BUS	-15VDC			B
E48	A2XA14-36	11	BUS-E48	11	BUS	+15VDC			
947*	A2XA14-51	14	ADAPTER 947	14	188 SHLD	GND		COAX	
947*	A2XA14-52	14	ADAPTER 947	14	189 CTR	R15M1X		COAX	
947*	A2XA14-53	14	ADAPTER 947	14	183 SHLD	GND		COAX	
E53	A2XA14-53	11	GND BUS-E53	11	BUS	GND			
E54	A2XA14-54	11	GND BUS-E54	11	BUS	GND			
E55	A2XA14-55	11	GND BUS-E55	11	BUS	GND			
861*	A2XA14-56	15	ADAPTER E61	15	188 SHLD	GND		COAX	
E56	A2XA14-56	11	GND BUS-E56	11	BUS	GND			
861*	A2XA14-57	15	ADAPTER 861	15	188 CTR	RVCCNT		COAX	

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1070 A 80063 54-A-75[illegible]28 F

SHEET 39

WIRE NO.	FROM END	TERM	ENC	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
861*A2XA14-5E		15	ADAPTER	861 15	188 SHLD	GND	COAX		
860*A2XA14-65		15	ADAPTER	860 15	188 SHLD	GND	COAX		
860*A2XA14-66		15	ADAPTER	860 15	188 CTR	RVCO	COAX		
860*A2XA14-67		15	ADAPTER	860 15	188 SHLD	GND	COAX		
E64 A2XA14-7C		11	BLS-E64	11	BLS	-15VDC			
E48 A2XA14-72		11	BLS-E48	11	BLS	+15VDC			
903*A2XA15-C2		14	ADAPTER	903 14	188 SHLD	GND	COAX		
903*A2XA15-C3		14	ADAPTER	903 14	188 CTR	RM1X0	COAX		
903*A2XA15-C4		14	ADAPTER	903 14	188 SHLD	GND	COAX		
947*A2XA15-C5		14	ADAPTER	947 14	188 SHLD	GND	COAX		
947*A2XA15-C6		14	ADAPTER	947 14	188 CTR	R15M1X	COAX		
947*A2XA15-C7		14	ADAPTER	947 14	188 SHLD	GND	COAX		
904*A2XA15-C8		14	ADAPTER	904 14	188 SHLD	GND	COAX		
904*A2XA15-C9		14	ADAPTER	904 14	188 CTR	R45M1X	COAX		
904*A2XA15-1C		14	ADAPTER	904 14	188 SHLD	GND	COAX		
E53 A2XA15-17		11	GND BUS-853	11	BLS	GND			
854 A2XA15-18		11	GND BLS-854	11	BUS	GND			
855 A2XA15-19		11	GND BLS-855	11	BUS	GND			
E56 A2XA15-20		11	GND BLS-856	11	BUS	GND			
864 A2XA15-34		11	BLS-E64	1	BLS	-15VDC			
848 A2XA15-3E		11	BLS-E48	11	BLS	+15VDC			
903*A2XA15-38		14	ADAPTER	903 14	188 SHLD	GND	COAX		
903*A2XA15-39		14	ADAPTER	903 14	188 CTR	RM1X0	COAX		
903*A2XA15-4C		14	ADAPTER	903 14	188 SHLD	GND	COAX		
947*A2XA15-41		14	ADAPTER	947 14	188 SHLD	GND	COAX		
947*A2XA15-42		14	ADAPTER	947 14	188 CTR	R15M1X	COAX		
947*A2XA15-43		14	ADAPTER	947 14	188 SHLD	GND	COAX		
904*A2XA15-44		14	ADAPTER	904 14	188 SHLD	GND	COAX		
904*A2XA15-45		14	ADAPTER	904 14	188 CTR	R45M1X	COAX		
904*A2XA15-4E		14	ADAPTER	904 14	188 SHLD	GND	COAX		
853 A2XA15-53		11	GND BLS-853	11	BLS	GND			
E54 A2XA15-54		11	GND BLS-E54	11	BLS	GND			
855 A2XA15-55		11	GND BLS-E55	11	BLS	GND			
E56 A2XA15-56		11	GND BLS-E56	11	BLS	GND			
E64 A2XA15-7C		11	BLS-E64	11	BLS	-15VDC			
848 A2XA15-72		11	BLS-E48	11	BLS	+15VDC			
909*A2XA16-12		14	ADAPTER	909 14	188 SHLD	GND	COAX		
909*A2XA16-13		14	ADAPTER	909 14	188 CTR	R45MA	COAX		
909*A2XA16-14		14	ADAPTER	909 14	188 SHLD	GND	COAX		
E53 A2XA16-17		11	GND BLS-853	11	BLS	GND			

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
854	A2XA16-1B	11	GND BUS-854	11	BUS	GND			
855	A2XA16-1C	11	GND BUS-855	11	BUS	GND			
856	A2XA16-2C	11	GND BUS-856	11	BUS	GND			
904*	A2XA16-21	14	ADAPTER 904	14	188 SHLD	GND	COAX		
904*	A2XA16-22	14	ADAPTER 904	14	188 CTR	R45M1X	COAX		
9C4*	A2XA16-23	14	ADAPTER 904	14	188 SHLD	GND	COAX		
902*	A2XA16-2A	14	ADAPTER 902	14	188 SHLD	GND	COAX		
902*	A2XA16-3C	14	ADAPTER 902	14	188 CTR	R45MVCO	COAX		
9C2*	A2XA16-31	14	ADAPTER 902	14	188 SHLD	GND	COAX		
864	A2XA16-34	11	BUS-864	11	BUS	-15VDC			
848	A2XA16-3E	11	BUS-848	11	BUS	+15VDC			
909*	A2XA16-48	14	ADAPTER 909	14	188 SHLD	GND	COAX		
9C9*	A2XA16-49	14	ADAPTER 909	14	188 CTR	R45MA	COAX		
9C9*	A2XA16-5C	14	ADAPTER 909	14	188 SHLD	GND	COAX		
853	A2XA16-53	11	GND BUS-853	11	BUS	GND			
854	A2XA16-54	11	GND BUS-854	11	BUS	GND			
855	A2XA16-55	11	GND BUS-855	11	BUS	GND			
856	A2XA16-56	11	GND BUS-856	11	BUS	GND			
9C4*	A2XA16-57	14	ADAPTER 904	14	188 SHLD	GND	COAX		
904*	A2XA16-5E	14	ADAPTER 904	14	188 CTR	R45M1X	COAX		
904*	A2XA16-65	14	ADAPTER 904	14	188 SHLD	GND	COAX		
902*	A2XA16-66	14	ADAPTER 902	14	188 SHLD	GND	COAX		
902*	A2XA16-6E	14	ADAPTER 902	14	188 CTR	R45MVCO	COAX		
902*	A2XA16-67	14	ADAPTER 902	14	188 SHLD	GND	COAX		
864	A2XA16-7C	11	BUS-864	11	BUS	-15VDC			
848	A2XA16-72	11	BUS-848	11	BUS	+15VDC			
853	A2XA17-17	11	GND BUS-853	11	BUS	GND			B
854	A2XA17-18	11	GND BUS-854	11	BUS	GND			B
855	A2XA17-19	11	GND BUS-855	11	BUS	GND			B
856	A2XA17-2C	11	GND BUS-856	11	BUS	GND			B
864	A2XA17-34	11	BUS-864	11	BUS	-15VDC			B
848	A2XA17-3E	11	BUS-848	11	BUS	+15VDC			B
853	A2XA17-53	11	GND BUS-853	11	BUS	GND			B
854	A2XA17-54	11	GND BUS-854	11	BUS	GND			B
855	A2XA17-55	11	GND BUS-855	11	BUS	GND			B
856	A2XA17-5E	11	GND BUS-856	11	BUS	GND			B
864	A2XA17-7C	11	BUS-864	11	BUS	-15VDC			B
848	A2XA17-72	11	BUS-848	11	BUS	+15VDC			B
850	A2XA18-02	11	BUS-850	11	BUS	+5VDC			
705	A2XA18-C4	11	BUS-705	11	BUS	-5VDC			

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1070 A 80063 SM-A-759528 F

SHEET 41

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
E53	A2XA18-17	11	GND BUS-853	11	BUS	GND			
854	A2XA18-18	11	GND BUS-854	11	BUS	GND			
E55	A2XA18-19	11	GND BUS-855	11	BUS	GND			
1014*	A2XA18-2C	6	A1JC1-38	6	30SCL BK	RSYNGND	TW2-859		B
E56	A2XA18-2C	11	GND BUS-856	11	BUS	GND			
900	A2XA18-21	6	A2XA18-23	6	30SCL W	RSAMP			
1020	A2XA18-22	6	A2XA20-23	6	30SCL W	RDUMP			B
900*	A2XA18-23	6	A2XA18-21	6	30SCL W	RSAMP			
901	A2XA18-23	6	A2XA23-35	6	30SCL W	RSAMP			
1014*	A2XA18-25	6	A1JC1-37	6	30SCL W	RSYNTST	TW2-1014		B
902*	A2XA18-29	14	ADAPTER 902	14	188 SHLD	GND	COAX		
902*	A2XA18-3C	14	ADAPTER 902	14	188 CTR	R45MVCO	COAX		
902*	A2XA18-31	14	ADAPTER 902	14	188 SHLD	GND	COAX		
864	A2XA18-34	11	BUS-864	11	BUS	-15VDC			
848	A2XA18-36	11	BUS-848	11	BUS	+15VDC			
850	A2XA18-38	11	BUS-850	11	BUS	+5VDC			
705	A2XA18-4C	11	BUS-705	11	BUS	-5VDC			
853	A2XA18-53	11	GND BUS-853	11	BUS	GND			
854	A2XA18-54	11	GND BUS-854	11	BUS	GND			
855	A2XA18-55	11	GND BUS-855	11	BUS	GND			
856	A2XA18-56	11	GND BUS-856	11	BUS	GND			
902*	A2XA18-65	14	ADAPTER 902	14	188 SHLD	GND	COAX		B
902*	A2XA18-66	14	ADAPTER 902	14	188 CTR	R45MVCO	COAX		B
902*	A2XA18-67	14	ADAPTER 902	14	188 SHLD	GND	COAX		
864	A2XA18-7C	11	BUS-864	11	BUS	-15VDC			
848	A2XA18-72	11	BUS-848	11	BUS	+15VDC			
850	A2XA19-C2	11	BUS-850	11	BUS	+5VDC			B
705	A2XA19-C4	11	BUS-705	11	BUS	-5VDC			B
853	A2XA19-17	11	GND BUS-853	11	BUS	GND			B
854	A2XA19-18	1011	GND BUS-854	11	BUS	GND			B
855	A2XA19-19	11	GND BUS-855	11	BUS	GND			B
856	A2XA19-20	11	GND BUS-856	11	BUS	GND			B
864	A2XA19-34	11	BUS-864	11	BUS	-15VDC			B
848	A2XA19-36	11	BUS-848	11	BUS	+15VDC			B
850	A2XA19-38	11	BUS-850	11	BUS	+5VDC			B
705	A2XA19-4C	11	BUS-705	11	BUS	-5VDC			B
853	A2XA19-53	11	GND BUS-853	11	BUS	GND			B
854	A2XA19-54	11	GND BUS-854	11	BUS	GND			B
855	A2XA19-55	11	GND BUS-855	11	BUS	GND			B
856	A2XA19-56	11	GND BUS-856	11	BUS	GND			B

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1C7C A 8CC63 SM-A-759628 F

SHEET 42

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NCDE	NOTE	REMARKS	REV
E64	A2XA19-70	11	BUS-E64	11	BLS	-15VDC			B
E48	A2XA19-72	11	BLS-E48	11	BUS	+15VDC			B
E50	A2XA20-C2	11	BUS-E50	11	BLS	+5VDC			
705	A2XA20-C4	11	BLS-705	11	BUS	-5VDC			
1027*	A2XA20-C6	6	A2XA11-34	6	30SCL W	RXSYNRT		TW2-1027	B
1019	A2XA20-C7	6	A2XA21-21	6	30SCL W	RTCXOGND			B
1026*	A2XA20-C8	6	A2XA11-15	6	30SCL W	RXSYNRC		TW2-1026	B
9C5	A2XA20-11	6	A2XA24-46	6	30SCL W	RXMX1			
989	A2XA20-12	6	A2XA24-24	6	30SCL W	RXMX4			B
9C6	A2XA20-14	6	A2XA24-60	6	30SCL W	RXMX2			
9C7	A2XA20-15	6	A2XA24-59	6	30SCL W	RXMX8			
853	A2XA20-17	11	GND BLS-853	11	BUS	GND			
854	A2XA20-18	11	GND BLS-854	11	BLS	GND			
855	A2XA20-19	11	GND BLS-855	11	BUS	GND			
856	A2XA20-20	11	GND BLS-856	11	BLS	GND			
1020*	A2XA20-23	6	A2XA18-22	6	30SCL W	RDUMP			B
910	A2XA20-27	6	A2XA23-39	6	30SCL W	R10100KT			
896	A2XA20-28	6	A2XA21-14	6	30SCL W	RM1XD		TW2-896	
896	A2XA20-29	6	A2XA21-15	6	30SCL BK	RM1XDGND		TW2-896	
911	A2XA20-30	6	A2XA23-41	6	30SCL W	R100K1MT			
899	A2XA20-31	6	A2XA23-42	6	30SCL W	R1-10MT			
E64	A2XA20-34	11	BLS-E64	11	BLS	-15VDC			
E48	A2XA20-36	11	BLS-E48	11	BUS	+15VDC			
1026*	A2XA20-37	7	A2XA11-37	7	30SCL BK	GND		TW2-1026	B
1027*	A2XA20-37	7	A2XA11-37	7	30SCL BK	GND		TW2-1027	B
E50	A2XA20-38	11	BLS-E50	11	BUS	+5VDC			
705	A2XA20-40	11	BLS-705	11	BLS	-5VDC			
853	A2XA20-53	11	GND BLS-853	11	BUS	GND			
854	A2XA20-54	11	GND BLS-854	11	BLS	GND			
E55	A2XA20-55	11	GND BLS-855	11	BUS	GND			
856	A2XA20-56	11	GND BLS-856	11	BLS	GND			
864	A2XA20-70	11	BUS-E64	11	BLS	-15VDC			
848	A2XA20-72	11	BUS-E48	11	BLS	+15VDC			
E50	A2XA21-C2	11	BUS-E50	11	BLS	+5VDC			
705	A2XA21-C4	11	BLS-705	11	BLS	-5VDC			
9C3*	A2XA21-C6	14	ADAPTER 903	14	188 SHLD	GND		COAX	
9C3*	A2XA21-C7	14	ADAPTER 903	14	188 CTR	RM1XD		COAX	
9C3*	A2XA21-C8	14	ADAPTER 903	14	188 SHLD	GND		COAX	
896*	A2XA21-14	6	A2XA20-28	6	30SCL W	RM1XD		TW2-896	
896*	A2XA21-15	6	A2XA20-29	6	30SCL BK	RM1XDGND		TW2-896	

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
853	A2XA21-17	11	GND BUS-853	11	BUS	GND			
854	A2XA21-18	11	GND BUS-854	11	BUS	GND			
855	A2XA21-19	11	GND BUS-855	11	BUS	GND			
856	A2XA21-2C	11	GND BUS-856	11	BUS	GND			
1019*	A2XA21-21	6	A2XA2C-C7	6	30SCL W	RTCXCGND			B
864	A2XA21-34	11	BUS-864	11	BUS	-15VDC			
848	A2XA21-3E	11	BUS-848	11	BUS	+15VDC			
850	A2XA21-38	11	BUS-850	11	BUS	+5VDC			
705	A2XA21-4C	11	BUS-705	11	BUS	-5VDC			
SC3*	A2XA21-42	14	ADAPTER SC3	14	188 SHLD	GND	COAX		
S03*	A2XA21-43	14	ADAPTER SC3	14	188 CTR	RMIXO	COAX		
S03*	A2XA21-44	14	ADAPTER 903	14	188 SHLD	GND	COAX		
853	A2XA21-53	11	GND BUS-853	11	BUS	GND			
854	A2XA21-54	11	GND BUS-854	11	BUS	GND			
855	A2XA21-55	11	GND BUS-855	11	BUS	GND			
856	A2XA21-56	11	GND BUS-856	11	BUS	GND			
864	A2XA21-7C	11	BUS-864	11	BUS	-15VDC			
848	A2XA21-72	11	BUS-848	11	BUS	+15VDC			
850	A2XA22-C2	11	BUS-850	11	BUS	+5VDC			B
850	A2XA22-38	11	BUS-850	11	BUS	+5VDC			B
32	A2XA23-C1	11	BUS-32	11	BUS	GND			
862	A2XA23-C1	11	GND BUS-862	11	BUS	GND			
850	A2XA23-02	11	BUS-850	11	BUS	+5VDC			
906*	A2XA23-C3	6	A1J03-03	6	30SCL W	R10-100K			
1001*	A2XA23-C5	6	A1J02-05	6	30SCL W	R100K-1M			B
1002*	A2XA23-C6	6	A1JC3-C4	6	30SCL W	R1-10M			B
9C9*	A2XA23-C7	14	ADAPTER 909	14	188 SHLD	GND	COAX		
909*	A2XA23-C8	14	ADAPTER 909	14	188 CTR	R45MA	COAX		
SC9*	A2XA23-C9	14	ADAPTER 909	14	188 SHLD	GND	COAX		
915	A2XA23-14	6	A2XA24-26	6	30SCL W	RXPD0-2			
916	A2XA23-15	6	A2XA24-62	6	30SCL W	RXPD0-4			
917	A2XA23-16	6	A2XA24-67	6	30SCL W	RXPD0-8			
937	A2XA23-22	6	A2XA24-71	6	30SCL W	RXMPD-8			
935	A2XA23-23	6	A2XA24-29	6	30SCL W	RXMPD-2			
930	A2XA23-24	6	A2XA24-57	6	30SCL W	RXPD4-1			
932	A2XA23-25	6	A2XA24-48	6	30SCL W	RXPD4-4			
920	A2XA23-27	6	A2XA24-64	6	30SCL W	RXPD1-4			
918	A2XA23-28	6	A2XA24-33	6	30SCL W	RXPD1-1			
927	A2XA23-3C	6	A2XA24-45	6	30SCL W	RXPD3-2			
929	A2XA23-31	6	A2XA24-55	6	30SCL W	RXPD3-8			

Table B-1. Synthesizer and Bit Synchronizer, Wire List - Continued

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
923	A2XA23-22	6	A2XA24-C7	6	30SCL W	RXPD2-2			
913	A2XA23-23	6	A2XA24-12	6	30SCL W	RLDPGM			
901*	A2XA23-25	6	A2XA18-23	6	30SCL W	RSAMP			
32	A2XA23-27	11	BUS-32	11	BUS	GND			
862	A2XA23-37	11	GND BUS-862	11	BUS	GND			
850	A2XA23-38	11	BUS-850	11	BUS	+5VDC			
910*	A2XA23-39	6	A2XA2C-27	6	30SCL W	R10100KT			
911*	A2XA23-41	6	A2XA2C-30	6	30SCL W	R100K1MT			
899*	A2XA23-42	6	A2XA20-31	6	30SCL W	R1-10MT			
9C9*	A2XA23-43	14	ADAPTER 9C9	14	188 SHLD	GND	COAX		
9C9*	A2XA23-44	14	ADAPTER 9C9	14	188 CTR	R45MA	COAX		
909*	A2XA23-45	14	ADAPTER 909	14	188 SHLD	GND	COAX		
914	A2XA23-57	6	A2XA24-31	6	30SCL W	RXPD0-1			
936	A2XA23-58	6	A2XA24-61	6	30SCL W	RXMPD-4			
934	A2XA23-59	6	A2XA24-35	6	30SCL W	RXMPD-1			
931	A2XA23-60	6	A2XA24-11	6	30SCL W	RXPD4-2			
933	A2XA23-61	6	A2XA24-21	6	30SCL W	RXPD4-8			
921	A2XA23-62	6	A2XA24-32	6	30SCL W	RXPD1-8			
919	A2XA23-63	6	A2XA24-28	6	30SCL W	RXPD1-2			
926	A2XA23-65	6	A2XA24-C3	6	30SCL W	RXPD3-1			
928	A2XA23-66	6	A2XA24-13	6	30SCL W	RXPD3-4			
922	A2XA23-67	6	A2XA24-39	6	30SCL W	RXPD2-1			
924	A2XA23-68	6	A2XA24-C9	6	30SCL W	RXPD2-4			
925	A2XA23-69	6	A2XA24-C6	6	30SCL W	RXPD2-8			
32	A2XA24-C1	11	BUS-32	11	BUS	GND			
862	A2XA24-C1	11	GND BUS-862	11	BUS	GND			
1021*	A2XA24-C2	7	A1J03-C2	6	30SCL R	+5VDC			B
850	A2XA24-C2	11	BUS-850	11	BUS	+5VDC			B
926*	A2XA24-C3	6	A2XA23-65	6	30SCL W	RXPD3-1			
873*	A2XA24-C5	6	A1J03-24	6	30SCL W	RX9-3-1			
925*	A2XA24-C6	6	A2XA23-69	6	30SCL W	RXPD2-8			
923*	A2XA24-C7	6	A2XA23-32	6	30SCL W	RXPD2-2			
870*	A2XA24-C8	6	A1J03-19	6	30SCL W	RX9-2-2			
924*	A2XA24-C9	6	A2XA23-68	6	30SCL W	RXPD2-4			
879*	A2XA24-1C	6	A1J03-36	6	30SCL W	RX9-4-4			
931*	A2XA24-11	6	A2XA23-60	6	30SCL W	RXPD4-2			
913*	A2XA24-12	6	A2XA23-33	6	30SCL W	RLDPGM			
928*	A2XA24-13	6	A2XA23-66	6	30SCL W	RXPD3-4			
841*	A2XA24-14	6	A1J03-C6	6	30SCL W	R0-COM			
842*	A2XA24-15	6	A1J03-12	6	30SCL W	R1-COM			

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Table B-1. Synthesizer and Bit Synchronizer, Wire List - Continued

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
933*	A2XA24-21	6	A2XA23-61	6	30SCL W	RXPD4-8			
880*	A2XA24-22	6	A1JC3-37	6	30SCL W	RX9-4-8			
843*	A2XA24-23	6	A1JC3-17	6	30SCL W	R2-COM			
589*	A2XA24-24	6	A2XA20-12	6	30SCL W	RXMX4			B
539*	A2XA24-25	6	A1JC3-08	6	30SCL W	RX9-0-2			
515*	A2XA24-26	6	A2XA23-14	6	30SCL W	RXPD0-2			
540*	A2XA24-27	6	A1JC3-09	6	30SCL W	RX9-0-4			
519*	A2XA24-28	6	A2XA23-63	6	30SCL W	RXPD1-2			
935*	A2XA24-29	6	A2XA23-23	6	30SCL W	RXMPD-2			
543*	A2XA24-30	6	A1JC3-14	6	30SCL W	RX9-1-2			
514*	A2XA24-31	6	A2XA23-57	6	30SCL W	RXPD0-1			
971*	A2XA24-32	6	A2XA23-62	6	30SCL W	RXPD1-8			
518*	A2XA24-33	6	A2XA23-28	6	30SCL W	RXPD1-1			
934*	A2XA24-35	6	A2XA23-59	6	30SCL W	RXMPD-1			
32	A2XA24-37	11	BUS-22	11	BUS	GND			
862	A2XA24-37	11	GND BUS-862	11	BUS	GND			
850	A2XA24-38	11	BUS-850	11	BUS	+5VDC			B
522*	A2XA24-39	6	A2XA23-67	6	30SCL W	RXPD2-1			
869*	A2XA24-41	6	A1JC3-18	6	30SCL W	RX9-2-1			
871*	A2XA24-42	6	A1JC3-21	6	30SCL W	RX9-2-8			
574*	A2XA24-43	6	A1JC3-25	6	30SCL W	RX9-3-2			
546*	A2XA24-44	6	A1JC3-20	6	30SCL W	RX9-2-4			
527*	A2XA24-45	6	A2XA23-30	6	30SCL W	RXPD3-2			
505*	A2XA24-46	6	A2XA20-11	6	30SCL W	RXMX1			
578*	A2XA24-47	6	A1JC3-35	6	30SCL W	RX9-4-2			
532*	A2XA24-48	6	A2XA23-25	6	30SCL W	RXPD4-4			
544*	A2XA24-51	6	A1JC3-23	6	30SCL W	R3-COM			
545*	A2XA24-52	6	A1JC3-33	6	30SCL W	R4-COM			
575*	A2XA24-54	6	A1JC3-26	6	30SCL W	RX9-3-4			
529*	A2XA24-55	6	A2XA23-31	6	30SCL W	RXPD3-8			
576*	A2XA24-56	6	A1JC3-27	6	30SCL W	RX9-3-8			
530*	A2XA24-57	6	A2XA23-24	6	30SCL W	RXPD4-1			
577*	A2XA24-58	6	A1JC3-34	6	30SCL W	RX9-4-1			
507*	A2XA24-59	6	A2XA20-15	6	30SCL W	RXMX8			
506*	A2XA24-60	6	A2XA20-14	6	30SCL W	RXMX2			
936*	A2XA24-61	6	A2XA23-58	6	30SCL W	RXMPD-4			
516*	A2XA24-62	6	A2XA23-15	6	30SCL W	RXPD0-4			
944*	A2XA24-63	6	A1JC3-15	6	30SCL W	RX9-1-4			
520*	A2XA24-64	6	A2XA23-27	6	30SCL W	RXPD1-4			
538*	A2XA24-65	6	A1JC3-07	6	30SCL W	RX9-0-1			

Table B-1. Synthesizer and Bit Synchronizer, Wire List - Continued

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NCDE	NOTE	REMARKS	REV
941*A2XA24-66		6	A1JC3-10	6	3CSCL W	RX9-0-8			
917*A2XA24-67		6	A2XA23-16	6	30SCL W	RXPDO-8			
945*A2XA24-68		6	A1J03-16	6	3CSCL W	RX9-1-8			
942*A2XA24-69		6	A1J03-13	6	30SOL W	RX9-1-1			
937*A2XA24-71		6	A2XA23-22	6	3CSCL W	RXMPD-8			
1C51*A2XA3-36		6	A2XAC9-13	6	3CSCL O	+15VDC			
1046 BUS-03		1	W1-	12	E-2C BK	GND		GND PGT-03	B
1018*BUS-1018		11	A2XAC1-2C	11	BUS	GND			B
1018*BUS-101E		11	A2XAC1-56	11	BUS	GND			B
1018*BUS-1018		11	A2XAC2-2C	11	BUS	GND			B
1C18*BUS-1018		11	A2XAC2-56	11	BUS	GND			B
1018*BUS-1018		11	A2XA03-20	11	BUS	GND			B
1C18*BUS-1018		11	A2XAC3-56	11	BUS	GND			B
1018*BUS-101E		11	A2XA04-20	11	BUS	GND			B
1018*BUS-1018		11	A2XAC4-56	11	BUS	GND			B
1015 BUS-1018		1	W1-	12	E-20 BK	GND		GND PGT-1018 2/TERM	B
1C4*BUS-104		11	A2XAC5-01	11	BUS	GND			
104*BUS-104		11	A2XAC5-37	11	BUS	GND			
104*BUS-104		11	A2XAC6-01	11	BUS	GND			
104*BUS-104		11	A2XAC6-37	11	BUS	GND			
104*BUS-104		11	A2XAC7-01	11	BUS	GND			
104*BUS-104		11	A2XAC7-37	11	BUS	GND			
104*BUS-104		11	A2XAC8-01	11	BUS	GND			
104*BUS-104		11	A2XAC8-37	11	BUS	GND			
104*BUS-104		11	A2XAC9-01	11	BUS	GND			
104*BUS-104		11	A2XAC9-37	11	BUS	GND			
104*BUS-104		11	A2XA10-01	11	BUS	GND			
104*BUS-104		11	A2XA10-37	11	BUS	GND			
104*BUS-104		11	A2XA11-01	11	BUS	GND			B
104*BUS-104		11	A2XA11-37	11	BUS	GND			B
104*BUS-104		11	A2XA12-01	11	BUS	GND			B
104*BUS-104		11	A2XA12-37	11	BUS	GND			B
105 BUS-104		1	W1-	2	E-20 BK	GND		PWR PGT 104	B
1049*BUS-1049		11	A1XA21-02	11	BUS	+5VDC			B
1049*BUS-1049		11	A1XA21-38	11	BUS	+5VDC			B
1C49*BUS-1049		11	A1XA22-02	11	BUS	+5VDC			B
1049*BUS-1049		11	A1XA22-38	11	BUS	+5VDC			B
1049*BUS-1049		11	A1XA23-02	11	BUS	+5VDC			B
1C50 BUS-1049		1	J01-E	3	E-20 R	+5VDC		PWR PGT-1049 2/TERM	B

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Table B-1. Synthesizer and Bit Synchronizer, Wire List - Continued

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
106*BUS-106		11	A1XA21-04	11	BLS	-5VDC			
106*BLS-106		11	A1XA21-40	11	BLS	-5VDC			
106*BUS-106		11	A1XA22-04	11	BLS	-5VDC			
106*BUS-106		11	A1XA22-40	11	BUS	-5VDC			
106*BUS-106		11	A1XA23-04	11	BLS	-5VDC			
106*BUS-106		11	A1XA23-40	11	BLS	-5VDC			
858 BUS-106		1	J01-K	3	E-20 G	-5VDC		PWR PGT 2/TERM	
3*BUS-3		11	A1XAC1-01	11	BLS	GND			
3*BUS-3		11	A1XAC1-37	11	BLS	GND			
3*BLS-3		11	A1XAC2-01	11	BLS	GND			
3*BUS-3		11	A1XAC2-37	11	BLS	GND			
316*BUS-316		11	A2XAC1-36	11	BUS	+15VDC			
316*BUS-316		11	A2XAC1-72	11	BLS	+15VDC			
316*BUS-316		11	A2XAC2-36	11	BUS	+15VDC			
316*BUS-316		11	A2XAC2-72	11	BLS	+15VDC			
316*BUS-316		11	A2XAC3-36	11	BLS	+15VDC			
316*BUS-316		11	A2XAC3-72	11	BUS	+15VDC			
163 BUS-316		1	J01-F	3	E-20 D	+15VDC		PWR PGT 2/TERM	
318*BUS-318		11	A1XAC3-36	11	BLS	+15VDC			
318*BUS-318		11	A1XAC3-72	11	BLS	+15VDC			
318*BUS-318		11	A1XAC4-36	11	BLS	+15VDC			B
318*BUS-318		11	A1XAC4-72	11	BUS	+15VDC			B
318*BUS-318		11	A1XAC5-36	11	BLS	+15VDC			B
318*BUS-318		11	A1XAC5-72	11	BLS	+15VDC			B
318*BUS-318		11	A1XAC6-36	11	BLS	+15VDC			
318*BUS-318		11	A1XAC6-72	11	BLS	+15VDC			
318*BUS-318		11	A1XAC7-36	11	BLS	+15VDC			B
318*BUS-318		11	A1XAC7-72	11	BUS	+15VDC			B
318*BLS-318		11	A1XAC8-36	11	BLS	+15VDC			
318*BUS-318		11	A1XAC8-72	11	BLS	+15VDC			
318*BUS-318		11	A1XAC9-36	11	BUS	+15VDC			B
318*BUS-318		11	A1XAC9-72	11	BLS	+15VDC			B
318*BUS-318		11	A1XA10-36	11	BUS	+15VDC			
318*BUS-318		11	A1XA10-72	11	BUS	+15VDC			
318*BUS-318		11	A1XA11-36	11	BLS	+15VDC			
318*BUS-318		11	A1XA11-72	11	BUS	+15VDC			
318*BUS-318		11	A1XA12-36	11	BUS	+15VDC			B
318*BLS-318		11	A1XA12-72	11	BLS	+15VDC			B
318*BUS-318		11	A1XA13-36	11	BLS	+15VDC			B
318*BLS-318		11	A1XA13-72	11	BLS	+15VDC			B

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Table B-1. Synthesizer and Bit Synchronizer, Wire List - Continued

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM		REF NODE	NOTE	REMARKS	REV
318*	BUS-318	11	A1XA14-36	11	BUS		+15VDC			B
318*	BUS-318	11	A1XA14-72	11	BUS		+15VDC			B
318*	BUS-318	11	A1XA15-36	11	BUS		+15VDC			
318*	BUS-318	11	A1XA15-72	11	BUS		+15VDC			
163	BUS-318	1	J01-F	3	E-20	C	+15VDC		PWR PGT 2/TERM	
32*	BUS-32	11	A2XA23-01	11	BUS		GND			
32*	BUS-32	11	A2XA23-37	11	BUS		GND			
32*	BUS-32	11	A2XA24-01	11	BUS		GND			
32*	BUS-32	11	A2XA24-37	11	BUS		GND			
37	BUS-32	1	W1-	12	E-20	BK	GND		GND PGT	
34*	BUS-34	11	A1XA12-02	11	BUS		+5VDC			B
34*	BUS-34	11	A1XA12-38	11	BUS		+5VDC			B
34*	BUS-34	11	A1XA13-02	11	BUS		+5VDC			B
34*	BUS-34	11	A1XA13-38	11	BUS		+5VDC			B
34*	BUS-34	11	A1XA14-02	11	BUS		+5VDC			
34*	BUS-34	11	A1XA14-38	11	BUS		+5VDC			
34*	BUS-34	11	A1XA15-02	11	BUS		+5VDC			
34*	BUS-34	11	A1XA15-38	11	BUS		+5VDC			
34*	BUS-34	11	A1XA16-02	11	BUS		+5VDC			
34*	BUS-34	11	A1XA16-38	11	BUS		+5VDC			
34*	BUS-34	11	A1XA17-02	11	BUS		+5VDC			
34*	BUS-34	11	A1XA17-38	11	BUS		+5VDC			
157	BUS-34	1	J01-E	3	E-20	R	+5VDC		PWR PGT-34 2/TERM	B
35*	BUS-35	11	A2XAC2-02	11	BUS		+5VDC			
35*	BUS-35	11	A2XAC2-38	11	BUS		+5VDC			
35*	BUS-35	11	A2XAC3-02	11	BUS		+5VDC			
35*	BUS-35	11	A2XAC3-38	11	BUS		+5VDC			
35*	BUS-35	11	A2XAC4-02	11	BUS		+5VDC			
35*	BUS-35	11	A2XAC4-38	11	BUS		+5VDC			
35*	BUS-35	11	A2XAC5-02	11	BUS		+5VDC			
35*	BUS-35	11	A2XAC5-38	11	BUS		+5VDC			
35*	BUS-35	11	A2XAC6-02	11	BUS		+5VDC			
35*	BUS-35	11	A2XAC6-38	11	BUS		+5VDC			
35*	BUS-35	11	A2XAC7-02	11	BUS		+5VDC			
35*	BUS-35	11	A2XAC7-38	11	BUS		+5VDC			
35*	BUS-35	11	A2XAC8-02	11	BUS		+5VDC			
35*	BUS-35	11	A2XAC8-38	11	BUS		+5VDC			
35*	BUS-35	11	A2XAC9-02	11	BUS		+5VDC			
35*	BUS-35	11	A2XAC9-38	11	BUS		+5VDC			
35*	BUS-35	11	A2XA10-02	11	BUS		+5VDC			

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Table B-1. Synthesizer and Bit Synchronizer, Wire List - Continued

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR	ITEM	REF NODE	NOTE	REMARKS	REV
	35*BUS-35	11	A2XA1C-3E	11	BLS		+5VDC			
	35*BUS-35	11	A2XA11-02	11	BUS		+5VDC			B
	35*BUS-35	11	A2XA11-3E	11	BLS		+5VDC			B
	35*BUS-35	11	A2XA12-02	11	BUS		+5VDC			B
	35*BUS-35	11	A2XA12-3E	11	BLS		+5VDC			B
	35*BUS-35	11	A2XA13-02	11	BLS		+5VDC			B
	35*BUS-35	11	A2XA13-3E	11	BLS		+5VDC			B
158	BUS-35	1	J01-F	2	E-20	R	+5VDC		PWR PGT-35	B
	51*BUS-51	11	A1XAC3-17	11	BLS		GND			B
	51*BUS-51	11	A1XAC3-53	11	BLS		GND			B
	51*BUS-51	11	A1XAC4-17	11	BLS		GND			B
	51*BUS-51	11	A1XAC4-53	11	BLS		GND			B
	51*BUS-51	11	A1XAC5-17	11	BLS		GND			B
	51*BUS-51	11	A1XAC5-53	11	BUS		GND			B
	51*BUS-51	11	A1XAC6-17	11	BLS		GND			B
	51*BUS-51	11	A1XAC6-53	11	BLS		GND			B
	51*BUS-51	11	A1XAC7-17	11	BUS		GND			B
	51*BUS-51	11	A1XAC7-53	11	BUS		GND			B
	51*BUS-51	11	A1XAC8-17	11	BLS		GND			B
	51*BUS-51	11	A1XAC8-53	11	BLS		GND			B
	51*BUS-51	11	A1XAC9-17	11	BLS		GND			B
	51*BUS-51	11	A1XAC9-53	11	BLS		GND			B
	51*BUS-51	11	A1XA10-17	11	BUS		GND			B
	51*BUS-51	11	A1XA1C-53	11	BLS		GND			B
	51*BUS-51	11	A1XA11-17	11	BLS		GND			B
	51*BUS-51	11	A1XA11-53	11	BLS		GND			B
	51*BUS-51	11	A1XA12-17	11	BLS		GND			B
	51*BUS-51	11	A1XA12-53	11	BLS		GND			B
1044	BUS-51	1	W1-	12	E-20	BK	GND		GND PGT-51 2/TERM	B
	52*BUS-52	11	A1XAC3-18	11	BLS		GND			B
	52*BUS-52	11	A1XAC3-54	11	BLS		GND			B
	52*BUS-52	11	A1XAC4-18	11	BLS		GND			B
	52*BUS-52	11	A1XAC4-54	11	BLS		GND			B
	52*BUS-52	11	A1XAC5-18	11	BLS		GND			B
	52*BUS-52	11	A1XAC5-54	11	BLS		GND			B
	52*BUS-52	11	A1XAC6-18	11	BLS		GND			B
	52*BUS-52	11	A1XAC6-54	11	BLS		GND			B
	52*BUS-52	11	A1XAC7-18	11	BLS		GND			B
	52*BUS-52	11	A1XAC7-54	11	BLS		GND			B
	52*BUS-52	11	A1XAC8-18	11	BLS		GND			B

Table B-1. Synthesizer and Bit Synchronizer, Wire List - Continued

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM	REF NCDE	NOTE	REMARKS	REV
52	*BUS-52	11	A1XAC8-54	11	BLS	GND			B
52	*BUS-52	11	A1XAC9-18	11	BLS	GND			B
52	*BUS-52	11	A1XAC9-54	11	BLS	GND			B
52	*BUS-52	11	A1XA10-18	11	BUS	GND			B
52	*BUS-52	11	A1XA10-54	11	BLS	GND			B
52	*BUS-52	11	A1XA11-18	11	BUS	GND			B
52	*BUS-52	11	A1XA11-54	11	BLS	GND			B
52	*BUS-52	11	A1XA12-18	11	BUS	GND			B
52	*BUS-52	11	A1XA12-54	11	BLS	GND			B
1044	BUS-52	1	W1-	12	E-2C BK	GND		GND PGT-52 2/TERM	B
53	*BUS-53	11	A1XAC3-2C	11	BLS	GND			B
53	*BUS-53	11	A1XAC3-56	11	BUS	GND			B
53	*BUS-53	11	A1XAC4-2C	11	BLS	GND			B
53	*BUS-53	11	A1XAC4-56	11	BLS	GND			B
53	*BUS-53	11	A1XAC5-20	11	BLS	GND			B
53	*BUS-53	11	A1XAC5-56	11	BUS	GND			B
53	*BUS-53	11	A1XAC6-20	11	BLS	GND			B
53	*BUS-53	11	A1XAC6-56	11	BLS	GND			B
53	*BUS-53	11	A1XAC7-20	11	BLS	GND			B
53	*BUS-53	11	A1XAC7-56	11	BLS	GND			B
53	*BUS-53	11	A1XAC8-20	11	BLS	GND			B
53	*BUS-53	11	A1XAC8-56	11	BLS	GND			B
53	*BUS-53	11	A1XAC9-20	11	BUS	GND			B
53	*BUS-53	11	A1XAC9-56	11	BLS	GND			B
53	*BUS-53	11	A1XA10-20	11	BLS	GND			B
53	*BUS-53	11	A1XA10-56	11	BLS	GND			B
53	*BUS-53	11	A1XA11-20	11	BLS	GND			B
53	*BUS-53	11	A1XA11-56	11	BLS	GND			B
53	*BUS-53	11	A1XA12-20	11	BLS	GND			B
53	*BUS-53	11	A1XA12-56	11	BLS	GND			B
1045	BUS-53	1	W1-	12	E-2C BK	GND		GND PGT-53 2/TERM	B
55	*BUS-55	11	A1XAC3-19	11	BLS	GND			B
55	*BUS-55	11	A1XAC3-55	11	BLS	GND			B
55	*BLS-55	11	A1XAC4-19	11	BLS	GND			B
55	*BUS-55	11	A1XAC4-55	11	BLS	GND			B
55	*BUS-55	11	A1XAC5-19	11	BLS	GND			B
55	*BUS-55	11	A1XAC5-55	11	BLS	GND			B
55	*BUS-55	11	A1XAC6-19	11	BUS	GND			B
55	*BUS-55	11	A1XAC6-55	11	BLS	GND			B
55	*BUS-55	11	A1XAC7-19	11	BLS	GND			B

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1070 A 80063 SM-A-759628 F

SHEET 51

Table B-1. Synthesizer and Bit Synchronizer, Wire List - Continued

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
	55*BUS-55	11	A1XAC7-55	11	BLS	GND			B
	55*BUS-55	11	A1XAC8-19	11	BLS	GND			B
	55*BUS-55	11	A1XAC8-55	11	BLS	GND			B
	55*BUS-55	11	A1XAC9-19	11	BUS	GND			B
	55*BUS-55	11	A1XAC9-55	11	BLS	GND			B
	55*BUS-55	11	A1XA10-19	11	BUS	GND			B
	55*BUS-55	11	A1XA10-55	11	BUS	GND			B
	55*BUS-55	11	A1XA11-19	11	BUS	GND			B
	55*BUS-55	11	A1XA11-55	11	BLS	GND			B
	55*BUS-55	11	A1XA12-19	11	BLS	GND			B
	55*BUS-55	11	A1XA12-55	11	BLS	GND			B
1045	BUS-55	1	W1-	12	E-20	BK GND		GND PGT-55 2/TERM	B
	57*BUS-57	11	A1XA14-01	11	BLS	GND			B
	57*BUS-57	11	A1XA14-37	11	BLS	GND			B
	57*BUS-57	11	A1XA15-01	11	BLS	GND			B
	57*BUS-57	11	A1XA15-37	11	BUS	GND			B
	57*BUS-57	11	A1XA16-01	11	BUS	GND			
	57*BUS-57	11	A1XA16-37	11	BLS	GND			
	57*BUS-57	11	A1XA17-01	11	BUS	GND			
	57*BUS-57	11	A1XA17-37	11	BLS	GND			
1043	BLS-57	1	W1-	12	E-20	BK GND		GND PGT-57	B
	705*BUS-705	11	A2XA18-04	11	BUS	-5VDC			
	705*BLS-705	11	A2XA18-40	11	BUS	-5VDC			
	705*BLS-705	11	A2XA19-04	11	BLS	-5VDC			B
	705*BUS-705	11	A2XA19-40	11	BUS	-5VDC			B
	705*BLS-705	11	A2XA20-04	11	BLS	-5VDC			
	705*BUS-705	11	A2XA20-40	11	BLS	-5VDC			
	705*BUS-705	11	A2XA21-04	11	BUS	-5VDC			
	705*BUS-705	11	A2XA21-40	11	BLS	-5VDC			
160	BUS-705	1	J01-F	3	E-20	G -5VDC		PWR PGT 2/TERM	
	706*BLS-706	11	A2XAC4-04	11	BLS	-5VDC			
	706*BUS-706	11	A2XAC4-40	11	BLS	-5VDC			
	706*BUS-706	11	A2XAC5-04	11	BUS	-5VDC			
	706*BUS-706	11	A2XAC5-40	11	BLS	-5VDC			
160	BUS-706	1	J01-F	3	E-20	G -5VDC		PWR PGT 2/TERM	
	75*BUS-75	11	A1XAC6-34	11	BLS	-15VDC			
	75*BUS-75	11	A1XAC6-70	11	BLS	-15VDC			
	75*BUS-75	11	A1XAC7-34	11	BLS	-15VDC			B
	75*BUS-75	11	A1XAC7-70	11	BLS	-15VDC			B
	75*BLS-75	11	A1XAC8-34	11	BLS	-15VDC			

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1070 A 80063 SM-A-759528 F

SHEET 52

Table B-1. Synthesizer and Bit Synchronizer, Wire List - Continued

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
	75*BUS-75	11	A1XAC6-7C	11	BLS	-15VDC			
	75*BUS-75	11	A1XAC5-34	11	BLS	-15VDC			B
	75*BUS-75	11	A1XAC5-7C	11	BLS	-15VDC			B
	75*BUS-75	11	A1XA1C-34	11	BLS	-15VDC			
	75*BUS-75	11	A1XA1C-7C	11	BLS	-15VDC			
	75*BUS-75	11	A1XA11-34	11	BLS	-15VDC			
	75*BUS-75	11	A1XA11-7C	11	BUS	-15VDC			
	75*BUS-75	11	A1XA12-34	11	BLS	-15VDC			B
	75*BUS-75	11	A1XA12-7C	11	BLS	-15VDC			B
	75*BUS-75	11	A1XA13-34	11	BLS	-15VDC			B
	75*BLS-75	11	A1XA13-7C	11	BLS	-15VDC			B
	75*BUS-75	11	A1XA14-34	11	BUS	-15VDC			B
	75*BUS-75	11	A1XA14-7C	11	BLS	-15VDC			B
	75*BUS-75	11	A1XA15-34	11	BLS	-15VDC			
	75*BUS-75	11	A1XA15-7C	11	BLS	-15VDC			B
164	BLS-75	1	J01-S	3	E-2D V	-15VDC		PWR PGT 2/TERM	
	76*BUS-76	11	A2XAC1-34	11	BUS	-15VDC			
	76*BUS-76	11	A2XAC1-7C	11	BUS	-15VDC			
	76*BUS-76	11	A2XAC2-34	11	BUS	-15VDC			
	76*BUS-76	11	A2XAC2-7C	11	BUS	-15VDC			
	76*BUS-76	11	A2XAC3-34	11	BLS	-15VDC			
	76*BUS-76	11	A2XAC3-7C	11	BLS	-15VDC			
164	BUS-76	1	J01-S	3	E-2C V	-15VDC		PWR PGT 2/TERM	
	8*BUS-8	11	A1XAC1-C2	11	BLS	+5VDC			
	8*BUS-8	11	A1XAC1-38	11	BLS	+5VDC			
	8*BUS-8	11	A1XAC2-C2	11	BUS	+5VDC			
	8*BUS-8	11	A1XAC2-38	11	BLS	+5VDC			
	8*BUS-8	11	A1XAC3-C2	11	BUS	+5VDC			
	8*BUS-8	11	A1XAC3-38	11	BLS	+5VDC			
	8*BUS-8	11	A1XAC4-C2	11	BLS	+5VDC			B
	8*BUS-8	11	A1XAC4-38	11	BLS	+5VDC			B
	8*BUS-8	11	A1XAC5-C2	11	BLS	+5VDC			
	8*BUS-8	11	A1XAC5-38	11	BLS	+5VDC			
	8*BUS-8	11	A1XAC6-C2	11	BLS	+5VDC			
	8*BUS-8	11	A1XAC6-38	11	BLS	+5VDC			
156	BUS-8	1	J01-D	2	E-2C R	+5VDC		PWR PGT-8	B
	81*BUS-81	11	A1XA21-17	11	BLS	GND			B
	81*BLS-81	11	A1XA21-53	11	BLS	GND			B
	81*BUS-81	11	A1XA22-17	11	BLS	GND			B
	81*BLS-81	11	A1XA22-53	11	BLS	GND			B

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 107C A 80063 SM-A-759628 F

SHEET 53

Table B-1. Synthesizer and Bit Synchronizer, Wire List - Continued

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM		REF NODE	NOTE	REMARKS	REV
E50*BUS-850		11	A2XA22-02	11	BLS		+5VDC			B
E50*BUS-85C		11	A2XA22-38	11	BLS		+5VDC			B
E50*BUS-850		11	A2XA23-02	11	BLS		+5VDC			
E50*BUS-85C		11	A2XA23-38	11	BUS		+5VDC			
E50*BUS-85C		11	A2XA24-02	11	BLS		+5VDC			B
F50*BLS-850		11	A2XA24-38	11	BLS		+5VDC			B
159 BUS-85C		1	J01-J	2	E-2C	R	+5VDC	PWR PGT		B
86*BUS-86		11	A1XA21-18	11	BLS		GND			B
86*BUS-86		11	A1XA21-54	11	BLS		GND			B
P6*BUS-86		11	A1XA22-18	11	BLS		GND			B
86*BUS-86		11	A1XA22-54	11	BLS		GND			B
A6*BUS-86		11	A1XA23-18	11	BLS		GND			B
86*BLS-86		11	A1XA23-54	11	BLS		GND			B
1039 BUS-86		1	W1-	12	E-2D	BK	GND	GND PGT-86 2/TERM		B
E64*BLS-864		11	A2XA12-34	11	BLS		-15VDC			
E64*BUS-864		11	A2XA12-7C	11	BLS		-15VDC			
F64*BUS-864		11	A2XA13-34	11	BUS		-15VDC			
E64*BUS-E64		11	A2XA13-70	11	BUS		-15VDC			
E64*BUS-864		11	A2XA14-34	11	BLS		-15VDC			B
864*BUS-864		11	A2XA14-7C	11	BLS		-15VDC			
864*BLS-864		1	A2XA15-34	11	BLS		-15VDC			B
E64*BUS-864		11	A2XA15-7C	11	BLS		-15VDC			
8E4*BUS-864		11	A2XA16-34	11	BUS		-15VDC			
E64*BLS-E64		11	A2XA16-7C	11	BLS		-15VDC			
E64*BUS-864		11	A2XA17-34	11	BLS		-15VDC			B
E64*BUS-864		11	A2XA17-70	11	BUS		-15VDC			B
864*BUS-864		11	A2XA18-34	11	BLS		-15VDC			
864*BUS-864		11	A2XA18-70	11	BUS		-15VDC			
E64*BUS-864		11	A2XA19-34	11	BLS		-15VDC			B
E64*BUS-E64		11	A2XA19-70	11	BUS		-15VDC			B
E64*BUS-864		11	A2XA20-34	11	BLS		-15VDC			
864*BUS-864		11	A2XA20-70	11	BUS		-15VDC			
E64*BUS-864		11	A2XA21-34	11	BLS		-15VDC			
864*BUS-864		11	A2XA21-70	11	BLS		-15VDC			
43 BUS-864		1	J01-V	2	E-2C	V	-15VDC	PWR PGT		
89*BUS-89		11	A1XA21-19	11	BLS		GND			B
89*BUS-89		11	A1XA21-55	11	BLS		GND			B
89*BLS-89		11	A1XA22-19	11	BLS		GND			B
89*BUS-89		11	A1XA22-55	11	BLS		GND			B
89*BLS-89		11	A1XA23-19	11	BLS		GND			B

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1070 A 80C63 SM-A-759628 F

SHEET 55

Table B-1. Synthesizer and Bit Synchronizer, Wire List - Continued

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM		REF NODE	NOTE	REMARKS	REV
E50*BUS-850		11	A2XA22-02	11	BLS		+5VDC			B
E50*BUS-85C		11	A2XA22-38	11	BLS		+5VDC			B
E50*BUS-850		11	A2XA23-02	11	BLS		+5VDC			
E50*BUS-85C		11	A2XA23-38	11	BUS		+5VDC			
E50*BUS-85C		11	A2XA24-02	11	BLS		+5VDC			B
F50*BLS-850		11	A2XA24-38	11	BLS		+5VDC			B
159 BUS-E5C		1	J01-J	2	E-2C	R	+5VDC	PWR PGT		B
86*BUS-86		11	A1XA21-18	11	BLS		GND			B
86*BUS-E6		11	A1XA21-54	11	BLS		GND			B
P6*BUS-86		11	A1XA22-18	11	BLS		GND			B
86*BUS-86		11	A1XA22-54	11	BLS		GND			B
A6*BUS-86		11	A1XA23-18	11	BLS		GND			B
86*BLS-86		11	A1XA23-54	11	BLS		GND			B
1039 BUS-86		1	W1-	12	E-2D	BK	GND	GND PGT-86 2/TERM		B
E64*BLS-864		11	A2XA12-34	11	BLS		-15VDC			
E64*BUS-864		11	A2XA12-7C	11	BLS		-15VDC			
F64*BUS-864		11	A2XA13-34	11	BUS		-15VDC			
E64*BUS-E64		11	A2XA13-70	11	BUS		-15VDC			
E64*BUS-864		11	A2XA14-34	11	BLS		-15VDC			B
864*BUS-864		11	A2XA14-7C	11	BLS		-15VDC			
864*BLS-864		1	A2XA15-34	11	BLS		-15VDC			B
E64*BUS-864		11	A2XA15-7C	11	BLS		-15VDC			
8E4*BUS-864		11	A2XA16-34	11	BUS		-15VDC			
E64*BLS-E64		11	A2XA16-7C	11	BLS		-15VDC			
E64*BUS-864		11	A2XA17-34	11	BLS		-15VDC			B
E64*BUS-864		11	A2XA17-70	11	BUS		-15VDC			B
864*BUS-864		11	A2XA18-34	11	BLS		-15VDC			
864*BUS-864		11	A2XA18-70	11	BUS		-15VDC			
E64*BUS-864		11	A2XA19-34	11	BLS		-15VDC			B
E64*BUS-E64		11	A2XA19-70	11	BUS		-15VDC			B
E64*BUS-864		11	A2XA2C-34	11	BLS		-15VDC			
864*BUS-864		11	A2XA2C-70	11	BUS		-15VDC			
E64*BUS-864		11	A2XA21-34	11	BLS		-15VDC			
864*BUS-864		11	A2XA21-7C	11	BLS		-15VDC			
43 BUS-864		1	J01-V	2	E-2C	V	-15VDC	PWR PGT		
89*BUS-89		11	A1XA21-19	11	BLS		GND			B
89*BUS-89		11	A1XA21-55	11	BUS		GND			B
89*BLS-89		11	A1XA22-19	11	BLS		GND			B
89*BUS-89		11	A1XA22-55	11	BLS		GND			B
89*BLS-89		11	A1XA23-19	11	BLS		GND			B

Table B-1. Synthesizer and Bit Synchronizer, Wire List - Continued

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM		REF NODE	NOTE	REMARKS	REV
89*BUS-89		11	A1XA23-55	11	BUS		GND			B
1039 BUS-89		1	W1-	12	E-20	BK	GND		GND PGT-89 2/TERM	B
93*BUS-93		11	A2XAC1-19	11	BUS		GND			B
93*BUS-93		11	A2XAC1-55	11	BUS		GND			B
93*BUS-93		11	A2XAC2-19	11	BUS		GND			B
93*BUS-93		11	A2XAC2-55	11	BUS		GND			B
93*BUS-93		11	A2XAC3-19	11	BUS		GND			B
93*BUS-93		11	A2XAC3-55	11	BUS		GND			B
93*BUS-93		11	A2XAC4-19	11	BUS		GND			B
93*BUS-93		11	A2XAC4-55	11	BUS		GND			B
1015 BUS-93		1	W1-	12	E-20	BK	GND		GND PGT-93 2/TERM	B
95*BUS-95		11	A2XAC1-18	11	BUS		GND			B
95*BUS-95		11	A2XAC1-54	11	BUS		GND			B
95*BUS-95		11	A2XAC2-18	11	BUS		GND			B
95*BUS-95		11	A2XAC2-54	11	BUS		GND			B
95*BUS-95		11	A2XAC3-18	11	BUS		GND			B
95*BUS-95		11	A2XAC3-54	11	BUS		GND			B
95*BUS-95		11	A2XAC4-18	11	BUS		GND			B
95*BUS-95		11	A2XAC4-54	11	BUS		GND			B
1006 BUS-95		1	W1-	12	E-20	BK	GND		GND PGT-95 2/TERM	B
968*BUS-968		11	A1XAC3-C4	11	BUS		-5VDC			B
968*BUS-968		11	A1XAC3-40	11	BUS		-5VDC			B
969*BUS-968		1	BUS-E3	1	E-20	G	-5VDC		BUS TO BUS PGT	B
E58 BUS-968		1	J01-K	3	E-20	G	-5VDC		PWR PGT 2/TERM	B
97*BUS-97		11	A2XAC1-17	11	BUS		GND			B
97*BUS-97		11	A2XAC1-53	11	BUS		GND			B
97*BUS-97		11	A2XAC2-17	11	BUS		GND			B
97*BUS-97		11	A2XAC2-53	11	BUS		GND			B
97*BUS-97		11	A2XAC3-17	11	BUS		GND			B
97*BUS-97		11	A2XAC3-53	11	BUS		GND			B
97*BUS-97		11	A2XAC4-17	11	BUS		GND			B
97*BUS-97		11	A2XAC4-53	11	BUS		GND			B
1006 BUS-97		1	W1-	12	E-20	BK	GND		GND PGT-97 2/TERM	B
E53*GND BUS-E53		11	A2XA13-17	11	BUS		GND			
E53*GND BUS-E53		11	A2XA13-53	11	BUS		GND			
E53*GND BUS-E53		11	A2XA14-17	11	BUS		GND			
E53*GND BUS-E53		11	A2XA14-53	11	BUS		GND			
E53*GND BUS-E53		11	A2XA15-17	11	BUS		GND			
E53*GND BUS-E53		11	A2XA15-53	11	BUS		GND			
E53*GND BUS-E53		11	A2XA16-17	11	BUS		GND			

(SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

HIGHEST WIRE NUMBER IS 1010 A 80063 SM-A-759628 F

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Table B-1. Synthesizer and Bit Synchronizer, Wire List - Continued

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
853*GND	BUS-853	11	A2XA16-53	11	BLS	GND			
853*GND	BUS-853	11	A2XA17-17	11	BUS	GND			B
853*GND	BUS-853	11	A2XA17-53	11	BUS	GND			B
853*GND	BUS-853	11	A2XA18-17	11	BUS	GND			
853*GND	BUS-853	11	A2XA18-53	11	BLS	GND			
853*GND	BUS-853	11	A2XA19-17	11	BLS	GND			B
853*GND	BUS-853	11	A2XA19-53	11	BUS	GND			B
853*GND	BUS-853	11	A2XA2C-17	11	BLS	GND			
853*GND	BUS-853	11	A2XA2C-53	11	BUS	GND			
853*GND	BLS-853	11	A2XA21-17	11	BLS	GND			
853*GND	BUS-853	11	A2XA21-53	11	BLS	GND			
41 GND	BUS-853	1	W1-	12	E-20	BK GND		GND PGT 2/TERM	
854*GND	BUS-854	11	A2XA13-18	11	BLS	GND			
854*GND	BUS-854	11	A2XA13-54	11	BLS	GND			
854*GND	BUS-854	11	A2XA14-18	11	BLS	GND			
854*GND	BUS-854	11	A2XA14-54	11	BLS	GND			
854*GND	BUS-854	11	A2XA15-18	11	BUS	GND			
854*GND	BUS-854	11	A2XA15-54	11	BLS	GND			
854*GND	BUS-854	11	A2XA16-18	11	BLS	GND			
854*GND	BUS-854	11	A2XA16-54	11	BLS	GND			
854*GND	BUS-854	11	A2XA17-18	11	BUS	GND			B
854*GND	BUS-854	11	A2XA17-54	11	BUS	GND			B
854*GND	BUS-854	11	A2XA18-18	11	BUS	GND			
854*GND	BUS-854	11	A2XA18-54	11	BUS	GND			
854*GND	BUS-854	11	A2XA19-18	1011	BUS	GND			B
854*GND	BUS-854	11	A2XA19-54	11	BLS	GND			B
854*GND	BUS-854	11	A2XA2C-18	11	BLS	GND			
854*GND	BUS-854	11	A2XA2C-54	11	BUS	GND			
854*GND	BUS-854	11	A2XA21-18	11	BLS	GND			
854*GND	BUS-854	11	A2XA21-54	11	BLS	GND			
41 GND	BUS-854	1	W1-	12	E-2C	BK GND		GND PGT 2/TERM	
855*GND	BUS-855	11	A2XA13-19	11	BLS	GND			
855*GND	BUS-855	11	A2XA13-55	11	BUS	GND			
855*GND	BUS-855	11	A2XA14-19	11	BLS	GND			
855*GND	BUS-855	11	A2XA14-55	11	BUS	GND			
855*GND	BUS-855	11	A2XA15-19	11	BLS	GND			
855*GND	BUS-855	11	A2XA15-55	11	BLS	GND			
855*GND	BUS-855	11	A2XA16-19	11	BLS	GND			
855*GND	BUS-855	11	A2XA16-55	11	BLS	GND			
855*GND	BUS-855	11	A2XA17-19	11	BLS	GND			B

Table B-1. Synthesizer and Bit Synchronizer, Wire List - Continued

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM		REF NODE	NOTE	REMARKS	REV
E55*GND	BUS-E55	11	A2XA17-55	11	BLS		GND			B
E55*GND	BUS-E55	11	A2XA18-19	11	BUS		GND			
E55*GND	BUS-E55	11	A2XA18-55	11	BUS		GND			
855*GND	BUS-E55	11	A2XA19-19	11	BUS		GND			B
E55*GND	BUS-E55	11	A2XA19-55	11	BLS		GND			B
E55*GND	BUS-E55	11	A2XA20-19	11	BLS		GND			
E55*GND	BUS-E55	11	A2XA20-55	11	BUS		GND			
E55*GND	BUS-E55	11	A2XA21-19	11	BUS		GND			
855*GND	BUS-E55	11	A2XA21-55	11	BUS		GND			
42 GND	BUS-E55	1	W1-	12	E-20	BK	GND		GND PGT 2/TERM	
E56*GND	BUS-E56	11	A2XA13-20	11	BLS		GND			
856*GND	BUS-E56	11	A2XA13-56	11	BUS		GND			
E56*GND	BUS-E56	11	A2XA14-20	11	BLS		GND			
E56*GND	BUS-E56	11	A2XA14-56	11	BUS		GND			
E56*GND	BUS-E56	11	A2XA15-20	11	BLS		GND			
E56*GND	BUS-856	11	A2XA15-56	11	BLS		GND			
856*GND	BUS-E56	11	A2XA16-20	11	BUS		GND			
E56*GND	BUS-E56	11	A2XA16-56	11	BLS		GND			
E56*GND	BUS-856	11	A2XA17-20	11	BUS		GND			B
E56*GND	BUS-E56	11	A2XA17-56	11	BLS		GND			B
E56*GND	BUS-856	11	A2XA18-20	11	BUS		GND			
E56*GND	BUS-E56	11	A2XA18-56	11	BUS		GND			
856*GND	BUS-856	11	A2XA19-20	11	BLS		GND			B
E56*GND	BUS-856	11	A2XA19-56	11	BLS		GND			B
E56*GND	BUS-856	11	A2XA20-20	11	BUS		GND			
E56*GND	BUS-E56	11	A2XA20-56	11	BUS		GND			
E56*GND	BUS-856	11	A2XA21-20	11	BLS		GND			
E56*GND	BUS-E56	11	A2XA21-56	11	BUS		GND			
42 GND	BUS-856	1	W1-	12	E-20	BK	GND		GND PGT 2/TERM	
E62*GND	BUS-E62	11	A2XA23-01	11	BLS		GND			
862*GND	BUS-E62	11	A2XA23-37	11	BLS		GND			
862*GND	BUS-862	11	A2XA24-01	11	BLS		GND			
862*GND	BUS-E62	11	A2XA24-37	11	BUS		GND			
559 GND	BUS-E62	1	W1-	12	E-20	BK	GND		GND PGT-862	B
1050*J01-E		3	BUS-1049	1	E-20	R	+5VDC		PWR PGT-1049 2/TERM	B
152 J01-A		2	W1-	12	E-16	BK	GND		+5VDC RTN	
153 J01-C		2	W1-	12	E-20	BK	GND		-5VDC RTN	
156*J01-D		2	BUS-8	1	E-20	R	+5VDC		PWR PGT-8	B
157*J01-E		3	BUS-34	1	E-20	R	+5VDC		PWR PGT-34 2/TERM	B
160*J01-F		3	BUS-705	1	E-20	G	-5VDC		PWR PGT 2/TERM	

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Table B-1. Synthesizer and Bit Synchronizer, Wire List - Continued

WIRE NO.	FROM END	TERM	TO END	TERM	COLOR ITEM		REF NODE	NOTE	REMARKS	REV
160*J01-F		3	BUS-1C6	1	E-20	G	-5VDC		PWR PGT 2/TERM	
158*J01-H		2	BUS-35	1	E-20	R	+5VDC		PWR PGT-35	B
159*J01-J		2	BUS-E50	1	E-20	R	+5VDC		PWR PGT	B
858*J01-K		3	BUS-1C6	1	E-20	G	-5VDC		PWR PGT 2/TERM	
858*J01-K		3	BUS-968	1	E-20	G	-5VDC		PWR PGT 2/TERM	B
163*J01-P		3	BUS-316	1	E-20	O	+15VDC		PWR PGT 2/TERM	
163*J01-P		3	BUS-318	1	E-20	O	+15VDC		PWR PGT 2/TERM	
44*J01-R		2	BUS-E4E	1	E-20	O	+15VDC		PWR PGT	
164*J01-S		3	BUS-75	1	E-20	V	-15VDC		PWR PGT 2/TERM	
164*J01-S		3	BUS-7E	1	E-20	V	-15VDC		PWR PGT 2/TERM	
58 J01-T		2	J02-F	2	E-20	O	+15VDC			
43*J01-V		2	BUS-E64	1	E-20	V	-15VDC		PWR PGT	
154 J01-W		3	J02-A	2	E-20	BK	GND		+15VDCRTN 2/TERM	
154 J01-W		3	W1-	12	E-20	BK	GND		+15VDCRTN 2/TERM	B
155 J01-X		2	W1-	12	E-20	BK	GND		-15VDCRTN	
154*J02-A		2	J01-W	3	E-20	BK	GND		+15VDCRTN 2/TERM	
860*J02-B		2	ADAPTER	860	15 188	CTR	RVCO		COAX	
861*J02-H		2	ADAPTER	861	15 188	CTR	RVCONT		COAX	
161 *J02-K		2	ADAPTER	161	15 188	CTR	TVCO		COAX	B
162 *J02-M		2	ADAPTER	162	15 188	CTR	TVCONT		COAX	B
58*J02-P		2	J01-T	2	E-20	C	+15VDC			
1037*P01-CTR		13	ADAPTER	1037	15 188	CTR	LOSINB+		COAX	B
1037*P01-SHELL		13	ADAPTER	1037	15 188	SHLD	GND		COAX	B
150*W1-		12	A1J01-C1	7	E-24	BK	GND			
11*W1-		12	A2J01-C1	7	E-24	BK	GND			
1046*W1-		12	BUS-C3	1	E-20	BK	GND		GND PGT-03	B
1015*W1-		12	BUS-1C1E	1	E-20	BK	GND		GND PGT-1013 2/TERM	B
105*W1-		2	BUS-1C4	1	E-20	BK	GND		PWR PGT 104	B
37*W1-		12	BUS-32	1	E-20	BK	GND		GND PGT	
1044*W1-		12	BUS-51	1	E-20	BK	GND		GND PGT-51 2/TERM	B
1044*W1-		12	BUS-52	1	E-20	BK	GND		GND PGT-52 2/TERM	B
1045*W1-		12	BUS-53	1	E-20	BK	GND		GND PGT-53 2/TERM	B
1045*W1-		12	BUS-55	1	E-20	BK	GND		GND PGT-55 2/TERM	B
1043*W1-		12	BUS-57	1	E-20	BK	GND		GND PGT-57	B
1040*W1-		12	BUS-81	1	E-20	BK	GND		GND PGT-81 2/TERM	B
1040*W1-		1	BUS-82	1	E-20	BK	GND		GND PGT-82 2/TERM	B
1039*W1-		12	BUS-86	1	E-20	BK	GND		GND PGT-86 2/TERM	B
1039*W1-		12	BUS-89	1	E-20	BK	GND		GND PGT-89 2/TERM	B
1015*W1-		12	BUS-93	1	E-20	BK	GND		GND PGT-93 2/TERM	B
1006*W1-		12	BUS-95	1	E-20	BK	GND		GND PGT-95 2/TERM	B

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Table B-1. Synthesizer and Bit Synchronizer, Wire List - Continued

WIRE NO.	FROM END	FROM TERM	TO END	TO TERM	COLOR ITEM	REF NODE	NOTE	REMARKS	REV
1006*W1-		12	BLS-97	1	E-2C	BK GND		GND PGT-97 2/TERM	B
41*W1-		12	GND BLS-853	1	E-20	BK GND		GND PGT 2/TERM	
41*W1-		12	GND BLS-854	1	E-2C	BK GND		GND PGT 2/TERM	
42*W1-		12	GND BLS-855	1	E-2C	BK GND		GND PGT 2/TERM	
42*W1-		12	GND BLS-856	1	E-20	BK GND		GND PGT 2/TERM	
999*W1-		12	GND BLS-862	1	E-2C	BK GND		GND PGT-862	B
152*W1-		12	J01-A	2	E-16	BK GND		+5VDC RTN	
153*W1-		12	J01-C	2	E-20	BK GND		-5VDC RTN	
154*W1-		12	J01-B	3	E-20	BK GND		+15VDCRTN 2/TERM	B
155*W1-		12	J01-D	2	E-20	BK GND		-15VDCRTN	

('SYNTH & BIT SYNC)

SIZE CODE IDENT NO. REV

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Table B-2. Power Supply PS1 Wire List

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
J1	1	A1	35	18	W	
J1	2	A1	36	18	BK	
J1	3	A1	30	22	G	
A1	1	CR17	A	18	Y	
A1	2	C21	(-)	18	W/O	
A1	3	CR18	A	18	Y	
A1	4	CR19	A	18	BL	
A1	5	C22	(-)	18	V	
A1	6	CR20	A	18	BL	
A1	7	Q4	C	20	R	Twisted pair.
A1	8	C5	(+)	20	W/R	
A1	9	Q5	C	20	BK	Twisted pair.
A1	10	CR15	C	18	BR	
A1	10	CR11	A	24	BR	
A1	11	C20	(+)	18	W/BR	
A1	11	C18	(-)	24	W/BR	
A1	12	CR16	C	18	BR	
A1	12	CR12	A	24	BR	

Table B-2. Power Supply PS1 Wire List - Continued

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
A1	13	Q6	C	20	W	Twisted pair.
A1	14	C5	(+)	20	W/R	
A1	15	Q7	C	20	GY	Twisted pair.
A1	16	-				Not used.
A1	17	-				Not used.
A1	18	-				Not used.
A1	19	E4		22	GY	Twisted pair.
A1	20	A3	D	22	R	
A1	21	E3		22	W	Twisted pair.
A1	22	CR13	C	16	BK	2 wires.
A1	22	CR9	A	22	BK	
A1	23	C19	(+)	16	W/BK	2 wires.
A1	23	C17	(-)	22	W/BK	
A1	24	CR14	C	16	BK	2 wires.
A1	24	CR10	A	22	BK	
A1	25	E2		22	BK	Twisted pair.
A1	26	A3	A	22	R	
A1	27	E1		22	GY	Twisted pair.

Table B-2. Power Supply PS1 Wire List - Continued

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
A1	28	-				Not used.
A1	29	-				Not used.
A1	30	J1	3	22	G	
A1	31	-				Not used.
A1	32	-				Not used.
A1	33	-				Not used.
A1	34	CR3	C	18	W/BK	
A1	35	J1	1	18	W	
A1	36	J1	2	18	BK	
A1	37	CR2	C	18	W/BK	
CR2	A	C5	(-)	18	W/GY	
CR2	C	A1	37	18	W/BK	
CR3	C	A1	34	18	W/BK	
CR5	C	C5	(+)	18	W/R	
CR9	A	A1	22	22	BK	
CR10	A	A1	24	22	BK	
CR11	A	A1	10	24	BR	
CR12	A	A1	12	24	BR	

Table B-2. Power Supply PS1 Wire List - Continued

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
CR13	C	A1	22	16	BK	2 wires.
CR14	C	A1	24	16	BK	2 wires.
CR15	C	A1	10	18	BR	
CR16	C	A1	12	18	BR	
CR17	A	A1	1	18	Y	
CR18	A	A1	3	18	Y	
CR19	A	A1	4	18	BL	
CR20	A	A1	6	18	BL	
CR49	A	TP1		24	R	
CR49	A	C51	(+)	18	R	
CR49	G	P2	12	24	R	
CR49	C	C51	(-)	18	W/R	
CR50	A	C52	(+)	22	W/G	
CR50	G	P3	12	24	W/G	
CR50	C	TP2		24	G	
CR50	C	C52	(-)	22	G	
CR51	A	TP3		24	O	
CR51	A	C53	(+)	22	O	

Table B-2. Power Supply PSI Wire List - Continued

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
CR51	G	P2	1	24	O	
CR51	C	C53	(-)	22	W/O	
CR52	A	C54	(+)	22	W/V	
CR52	G	P3	1	24	W/V	
CR52	C	C54	(-)	22	V	
CR52	C	TP4		24	V	
C5	(+)	R1	A	22	W/R	
C5	(+)	CR5	C	18	W/R	
C5	(+)	A1	8	20	W/R	
C5	(+)	A1	14	20	W/R	
C5	(-)	Q6	E	20	W/G	
C5	(-)	CR2	A	18	W/G	
C5	(-)	Q5	E	20	W/G	
C5	(-)	A3	B	22	W/G	
C17	(+)	Q12	C	22	BK/BL	
C17	(+)	P2	14	22	BK/BL	
C17	(-)	A1	23	22	W/BK	
C18	(+)	Q13	C	24	BK/Y	

Table B-2. Power Supply PSI Wire List - Continued

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
C18	(+)	P3	14	24	BK/Y	
C18	(-)	A1	11	24	W/BR	
C19	(+)	A1	23	16	W/BK	2 wires.
C19	(+)	Q15	C	16	W/BK	
C19	(+)	Q17	C	16	W/BK	
C19	(-)	C51	(-)	16	W/R	2 wires.
C20	(+)	A1	11	18	W/BR	
C20	(+)	Q19	C	18	W/BR	
C20	(-)	C52	(-)	18	G	
C21	(+)	Q21	C	18	W/Y	
C21	(+)	P2	7	24	W/Y	
C21	(-)	A1	2	18	W/O	
C21	(-)	C53	(-)	18	W/O	
C22	(+)	Q23	C	18	V	
C22	(+)	P3	7	24	V	
C22	(-)	A1	5	18	V	
C22	(-)	C54	(-)	18	V	
C22	(-)	A1	5	18	V	

Table B-2. Power Supply PS1 Wire List - Continued

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
C51	(+)	E10		16	R	
C51	(+)	E13		16	R	
C51	(+)	CR49	A	18	R	
C51	(+)	P2	19	24	R	
C51	(+)	P2	20	24	R	Twisted pair.
C51	(+)	PS1P1	D	20	R	+5 V.
C51	(+)	PS1P1	E	20	R	+5 V.
C51	(+)	PS1P1	H	20	R	+5 V.
C51	(+)	PS1P1	H	20	R	+5 V.
C51	(+)	PS1P1	E	20	R	+5 V.
C51	(+)	PS1P1	J	20	R	+5 V.
C51	(+)	PS1P1	D	20	R	+5 V.
C51	(-)	C19	(-)	16	W/R	2 wires.
C51	(-)	CR49	C	18	W/R	
C51	(-)	P2	13	24	W/R	
C51	(-)	P2	15	24	W/R	Twisted pair.
C51	(-)	PS1P1	A	16	W/R	+5 V COM.
C51	(-)	PS1P1	B	16	W/R	+5 V COM.

Table B-2. Power Supply PS1 Wire List - Continued

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
C51	(-)	TP5		24	W/R	
C52	(+)	E5		18	W/G	
C52	(+)	CR50	A	22	W/G	
C52	(+)	P3	19	24	W/G	
C52	(+)	P3	20	24	W/G	Twisted pair.
C52	(+)	PS1P1	N	16	W/G	-5 V COM.
C52	(+)	PS1P1	C	16	W/G	-5 V COM.
C52	(-)	C20	(-)	18	G	
C52	(-)	CR50	C	22	G	
C52	(-)	P3	13	24	G	
C52	(-)	P3	15	24	G	Twisted pair.
C52	(-)	PS1P1	F	20	G	-5 V.
C52	(-)	PS1P1	K	20	G	-5 V.
C52	(-)	PS1P1	F	20	G	-5 V.
C53	(+)	E6		18	O	
C53	(+)	CR51	A	22	O	
C53	(+)	P2	10	24	O	
C53	(+)	P2	11	24	O	Twisted pair.

Table B-2. Power Supply PS1 Wire List - Continued

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
C53	(+)	PS1P1	P	20	O	+15 V.
C53	(+)	PS1P1	R	20	O	+15 V.
C53	(+)	PS1P1	P	20	O	+15 V.
C53	(+)	PS1P1	R	20	O	+15 V.
C53	(+)	PS1P1	T	20	O	+15 V.
C53	(+)	PS1P1	U	20	O	+15 V.
C53	(-)	C21	(-)	18	W/O	
C53	(-)	CR51	C	22	W/O	
C53	(-)	P2	4	24	W/O	
C53	(-)	P2	8	24	W/O	Twisted pair.
C53	(-)	PS1P1	W	16	W/O	+15 V COM.
C53	(-)	PS1P1	L	16	W/O	+15 V COM.
C54	(+)	E7		18	W/V	
C54	(+)	CR52	A	22	W/V	
C54	(+)	P3	10	24	W/V	
C54	(+)	P3	11	24	W/V	Twisted pair.
C54	(+)	PS1P1	X	16	W/V	-15 V COM.
C54	(+)	PS1P1	M	16	W/V	-15 V COM.

Table B-2. Power Supply PS1 Wire List - Continued

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
C54	(-)	C22	(-)	18	V	
C54	(-)	CR52	C	22	V	
C54	(-)	P3	4	24	V	
C54	(-)	P3	8	24	V	Twisted pair.
C54	(-)	PS1P1	V	20	V	-15 V.
C54	(-)	PS1P1	S	20	V	-15 V.
C54	(-)	PS1P1	V	20	V	-15 V.
C54	(-)	PS1P1	S	20	V	-15 V.
C51	(-)	C55				
C55		GND				
PS1P1	D	C51	(+)	20	R	+5 V.
PS1P1	E	C51	(+)	20	R	+5 V.
PS1P1	H	C51	(+)	20	R	+5 V.
PS1P1	H	C51	(+)	20	R	+5 V.
PS1P1	E	C51	(+)	20	R	+5 V.
PS1P1	J	C51	(+)	20	R	+5 V.
PS1P1	D	C51	(+)	20	R	+5 V.
PS1P1	A	C51	(+)	16	W/R	+5 V COM.

Table B-2. Power Supply PS1 Wire List - Continued

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
PS1P1	B	C51	(-)	16	W/R	+5 V COM.
PS1P1	N	C52	(+)	16	W/G	-5 V COM.
PS1P1	C	C52	(+)	16	W/G	-5 V COM.
PS1P1	F	C52	(-)	20	G	-5 V.
PS1P1	K	C52	(-)	20	G	-5 V.
PS1P1	F	C52	(-)	20	G	-5 V.
PS1P1	P	C53	(+)	20	O	+15 V.
PS1P1	R	C53	(+)	20	O	+15 V.
PS1P1	P	C53	(+)	20	O	+15 V.
PS1P1	R	C53	(+)	20	O	+15 V.
PS1P1	T	C53	(+)	20	O	+15 V.
PS1P1	U	C53	(+)	20	O	+15 V.
PS1P1	W	C53	(-)	16	W/O	+15 V COM.
PS1P1	L	C53	(-)	16	W/O	+15 V COM.
PS1P1	X	C54	(+)	16	W/V	-15 V COM.
PS1P1	M	C54	(+)	16	W/V	-15 V COM.
PS1P1	V	C54	(-)	20	V	-15 V.
PS1P1	S	C54	(-)	20	V	-15 V.

Table B-2. Power Supply PSI Wire List - Continued

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
PS1P1	V	C54	(-)	20	V	-15 V.
PS1P1	S	C54	(-)	20	V	-15 V.
TP1		CR49	A	24	R	
TP2		CR50	C	24	G	
TP3		CR51	A	24	O	
TP4		CR52	C	24	V	
TP5		C51	(-)	24	W/R	
Q4	C	A1	7	20	R	Twisted pair.
Q5	C	A1	9	20	BK	Twisted pair.
Q5	E	C5	(-)	18	W/G	
Q6	C	A1	13	20	W	Twisted pair.
Q7	C	A1	15	20	G	Twisted pair.
Q10	C	P2	5	24	R	
Q10	B	P2	6	24	W	
Q11	C	P3	5	24	O	
Q11	B	P3	6	24	Y	
Q12	C	C17	(+)	22	BK/BL	
Q12	B	P2	16	24	W/BL	

Table B-2. Power Supply PS1 Wire List - Continued

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
Q12	E	P2	17	24	Y	
Q13	C	C18	(+)	24	BK/Y	
Q13	B	P3	16	24	W	
Q13	E	P3	17	24	G	
Q13	E	Q19	B	24	G	
Q14	E	P2	18	24	W/BK	
Q15	C	C19	(+)	16	W/BK	
Q17	C	C19	(+)	16	W/BK	
Q19	C	C20	(+)	18	W/BR	
Q19	E	P3	18	24	W/BR	
Q19	B	Q13	E	24	G	
Q20	E	P2	9	24	G	
Q21	C	C21	(+)	18	W/Y	
Q22	E	P3	9	24	Y	
Q23	C	C22	(+)	18	V	
R1	A	C5	(+)	22	W/R	
R1	B	A3	E	22	W/R	
E1		A1	27	22	GY	Twisted pair. ▼

Table B-2. Power Supply PS1 Wire List - Continued

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
E2		A1	25	22	BK	
E3		A1	21	22	W	
E4		A1	19	22	G	Twisted pair.
E5		C52	(+)	18	W/G	
E6		C53	(+)	18	O	
E7		C54	(+)	18	W/V	
E10		C51	(+)	16	R	
E13		C51	(+)	16	R	
A3	A	A1	26	22	R	
A3	B	C5	(-)	22	W/G	
A3	C	-				Not used.
A3	D	A1	20	22	R	
A3	E	R1	B	22	W/R	
P2	1	CR51	G	24	O	
P2	2	-				Not used.
P2	3	-				Not used.
P2	4	C53	(-)	24	W/O	
P2	5	Q10	C	24	R	

Table B-2. Power Supply PS1 Wire List - Continued

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
E2		A1	25	22	BK	
E3		A1	21	22	W	
E4		A1	19	22	G	Twisted pair.
E5		C52	(+)	18	W/G	
E6		C53	(+)	18	O	
E7		C54	(+)	18	W/V	
E10		C51	(+)	16	R	
E13		C51	(+)	16	R	
A3	A	A1	26	22	R	
A3	B	C5	(-)	22	W/G	
A3	C	-				Not used.
A3	D	A1	20	22	R	
A3	E	R1	B	22	W/R	
P2	1	CR51	G	24	O	
P2	2	-				Not used.
P2	3	-				Not used.
P2	4	C53	(-)	24	W/O	
P2	5	Q10	C	24	R	

Table B-2. Power Supply PS1 Wire List - Continued

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
P2	6	Q10	B	24	W	
P2	7	C21	(+)	24	W/Y	
P2	8	C53	(-)	24	W/O	Twisted pair.
P2	9	Q20	E	24	G	
P2	10	C53	(+)	24	O	
P2	11	C53	(+)	24	O	Twisted pair.
P2	12	CR49	G	24	R	
P2	13	C51	(-)	24	W/R	
P2	14	C17	(+)	22	BK/BL	
P2	15	C51	(-)	24	W/R	Twisted pair.
P2	16	Q12	B	24	W/BL	
P2	17	Q12	E	24	Y	
P2	18	Q14	E	24	W/BK	
P2	19	C51	(+)	24	R	
P2	20	C51	(+)	24	R	
P3	1	CR52	G	24	W/V	
P3	2	-				Not used.
P3	3	-				Not used.

APPENDIX C

GLOSSARY OF TERMS

This appendix defines the mnemonics used to identify the signals carried between cards, card files, and subassemblies.

Table C-1. Glossary of Terms

Mnemonic	*Description*
A	External Jumper
AA	2R Clock To PN Sequence Generator
AAA	2R Clock To Encoder Complement
ALMRST	Alarm Reset
ALTCLK	Alternate Clock Output
ALTCLKT	Alternate Clock Test Output
ALTOUT	Alternate Data Output
ALTOUTT	Alternate Data Test Output
AUDALMI.2	Audible Alarm
B	2R Clock To Encoder True
BCKOUTT	Buffered Standard Clock Output True
BRD256C	Error Counter Load Count 256
BUFFOUTT	Standard Data Test Output
CBSDATC	Bypass Data
CLKONE	Drive To Clock B Indicator
CLKOUT	Standard Clock Output
CLKOUTT	Clock Output Circuit
CLKZER	Drive to Clock A Indicator
CLKOUTC	Standard Clock Output Complement
CLKOUTT	Clock Output Circuit
CMPATOC	Comparator Automatic Resync
COMPERRT	Comparator Error True
COMPCKC	Comparator Clock To Front Panel Connector
COMPACKT	Comparator Clock True
COMPDTC	Comparator Data Complement
COM POVC	Comparator Overflow Complement
CTN-11	External Jumper On Error Comparator
DACCLK	Clock Complement To D/A Converter, Loop Filter, and PN Sequence Generator
DATFD	Data From Decoder
DATFDCC	Data From External Decoder
DATFE	Symbols From Coder
DATFENC	Data From Encoder
DATONE	Drive To Data A Indicator
DATOUT	Standard Data Output
DATOUTT	Data To Output Circuits
DATTE	Data To Coder
DATTENT	Data To Internal Or External Coder
DATZER	Drive To Data B Indicator
DIFDECT	Differential Decoder Enable
DIFENCC	Differantial Encoder Enable
DISABL	+5 V FLTR
DSALMG	Disable Alarm
DSTBCK	Grount To Clock Input Of Divide By 37,500 Counter (Internal Clock)
ENCLKRC	Enable Clocked Data
ENOPERC	Enable Operate Mode
ENSTDRC	Enable Standard Data
ENTESTC	Enable Test Mode
EXTXGT	+5 V FLTR Jumper On Input Interface
ERRCNT	Error Count Enable
ERROUT	Error Pulse To Front Panel Connector
ERRSIG	Monitor Meter Return

Table C-1 Glossary of Terms-Continued

Mnemonic	*Description*
EXTALM1,2	External Alarm Contact Closure
EXTDECC	External Decoder Enable Complement
EXTDECT	External Decoder Enable True
EXTENCC	External Encoder Enable Complement
EXTENCT	External Encoder Enable True
ICFCLKT	ICF Clock
ICFDATT	ICF Test Data
ICFRLYE	Operate/Test Relay Control
ICFRYDAT	Receive ICF Data To Bit Detector
IFCOB75	Bipolar Output 75 Ohm Balanced
ICFOV50+	Bipolar NRZ Output 50 Ohm Unbalanced
ICFOU75 +	Bipolar Output 75 Ohm Unbalanced
ICFIB75__	75 Ohm Input (Balanced)
ICFIN50 t	50 Ohm Input (Unbalanced)
ICFIN75__	75 Ohm Input (Unbalanced)
ICF1	Decoded ICF Signals (before combining)
ICF2	Decoded ICF Signals (before combining)
INCLK	Standard Clock Input
INSTD	Standard Data Input
INTCLK	Internal Clock Output
INTCLKT	Test Output To PN Sequence Generator
LFMSBT	Transmit Data MSB To Loop Filter
LFOVERC	Transmit Loop Filter Overflow
LFTRANT	Transmit Data Transition To Loop Filter
LFUNDRT	Transmit Loop Filter Underflow
LOSINB +	LOS Input
LOSSLTC	Receive Bit Sync Loss Of Lock Indicator
LPFCLKT	Transmit Loop Filter Clock
MANSMPC	Comparator Manual Resync
MSBTD	Most Significant Bit To External Decoder
NODECC	No Decoding
NOENCC	No Encoding
OLCST	LOS Output
PULLUP+	+5 V On Counter Load Inputs
RBSBRC	Receive Bit Sync Bit Rate Complement
RBSBRT	Receive Bit Sync Bit Rate True
RBSBSSC	Frequency Control To Receive Frequency Synthesizer VCO
RBSDATT	Receive Bit Sync Data True
RCKFD	Receive Clock From External Decoder
RCKFDCT	R Clock From External Decoder
RCKTD	Receive Clock To External Decoder
RCKTDCT	Receive Clock To Decoder Interface True
RCKTE	Clock To Coder
RCLKTE +	R Clock To Encoder True
RDAC- I	Receive Loop Filler Output To D/A Converter
RDAC-2	
RDAC-3	
RDAC-4	
RDAC-5	
RDAC-6	
RDAC-7	
RDAC-8	
RDUMP	Receive Integrator Dump Signal
RLDPGM	Receive Load Program
RLFOVRC	Receive Loop Filter Overflow
RLFUNDT	Receive Loop Filter Underflow
RMIXD	30 $\pm$ 10 MHz To Receive Reference Divider
RMIXO	Receive Synthesizer 30 $\pm$ 10 MHz From Mixer/Output Amplifier
RSAMP	Receive Sample From Programmable Divider
RSIGNT	Receive Sign Bit To Loop filter
RSYNTST	Receive Test Of VCO Control Voltage To Meter
RTCXO	Receive Synthesizer 15 MHz TCXO Output
RTRANT	Receive Data Transition To Loop Filter
RVCO	Receive 15 MHz VCO Output
RVCONT	Control To Receive 15 MHz VCO

Table C-1. Glossary of Terms-Continued

Mnemonic	*Description*
RXBSLOL	Receive Bit Sync Loss Of Lock Indication
RXFAIL	Receive Section Fault Indication
RXMPD-1	Receive Programmable Divider Program Control
RXMPD-2	
RXMPD-4	
RXMPD-8	
RXMX1	Symbol Rate Switch Setting Between 50000 and 99999
RXMX2	Symbol Rate Switch Setting Between 25000 and 49999
RXMX4	Symbol Rate Switch Setting Between 12500 and 24999
RXMX8	Symbol Rate Switch Setting Between 10000 and 12499
RXPDO-1	Digit I (Least Significant) Of Counter Encoder Program Output
RX PDO-2	
RXPDO-4	(Receive Synthesizer)
RXPDO-8	
RXPDI-1	Digit 2 Of Counter Encoder Program Output (Receive
RXPDI-2	
RXPD1-4	Synthesizer)
RXPD1-8	
RXPD2-1	Digit 3 Of Counter Encoder Program Output (Receive
RXPD2-2	
RXPD2-4	Synthesizer)
RSPD2-8	
RSPD3-1	Digit 4 Of Counter Encoder Program Output (Receive
RXPD3-2	
RXPD3-4	Synthesizer)
RXPD3-8	
RXPD4-1	Digit 5 (Most Significant) Of Counter Encoder Program Output
RXPD4-2	
RXPD4-4	(Receive Synthesizer)
RXPD4-8	
RXPD5-1	Counter Encoder Multiplier Code To Synthesizer
RXPD5-2	
RXPD5-4	(Receive Synthesizer)
RXPD5-8	
RXSYNRC	Receive Bit Sync Clock Complement
RXSYNRT	Receive Bit Sync Clock True
RX9-0-1	Least Significant Symbol Rate Digit Includes 9’s Complement Of 20
RX9-0-2	Least Significant Symbol Rate Digit Includes 9’s Complement Of 2’
RX9-0-4	Least Significant Symbol Rate Digit Includes 9’s Complement Of 2’
RX9-0-8	Least Significant Symbol Rate Digit Includes 9’s Complement Of 21
RX9-1-1	Next Least Significant Symbol Rate Digit Includes 9’s Complement Of 2"
RX9-1-2	Next Least Significant Symbol Rate Digit Includes 9’s Complement Of 2’
RX9-1-4	Next Least Significant Symbol Rate Digit Includes 9’s Complement Of 2’
RX9-1-8	Next Least Significant Symbol Rate Digit Includes 9’s Complement Of 2’
RX9-2-1	MidD1e Significant Digit Symbol Rate Digit Includes 9’s Complement Of 2"
RX9-2-2	MidD1e Significant Digit Symbol Rate Digit Includes 9’s Complement Of 2’
RX9-2-4	MidD1e Significant Digit Symbol Rate Digit Includes 9’s Complement Of 2’
RX9-2-8	MidD1e Significant Digit Symbol Rate Digit Includes 9’s Complement Of 2’
RX9-3-1	Next Most Significant Symbol Rate Digit Includes 9’s Complement Of 2"
RX9-3-2	Next Most Significant Symbol Rate Digit Includes 9’s Complement Of 2’
RX9-3-4	Next Most Significant Symbol Rate Digit Includes 9’s Complement Of 2’
RX9-3-8	Next Most Significant Symbol Rate Digit Includes 9’s Complement Of 21
RX9-4-1	Most Significant Symbol Rate Digit Includes 9's Complement Of 2°
RX9-4-2	Most Significant Symbol Rate Digit Includes 9's Complement Of 2'
RX9-4-4	Most Significant Symbol Rate Digit Includes 9's Complement Of 2'
RX9-4-8	Most Significant Symbol Rate Digit Includes 9's Complement Of 2'
RO-COM	+5 V To Receive Symbol Rate S5
R1-COM	+5V To Receive Symbol Rate S4
R2-COM	+5 V To Receive Symbol Rate S3
R3-COM	+5 V To Receive Symbol Rate S2
R4-COM	+5 V To Receive Symbol Rate S1
R1-1OM	Symbol Rate Switch Selection Between I and 9.9999 MHz Complement
Rl-1OMT	Symbol Rate Switch Selection Between 1 and 9.9999 MHz True
R10-100K	Symbol Rate Switch Selection Between 19.2 and 99.999 kb/s
R100K-1M	Symbol Rate Switch Selection Between 100 and 999.99 kb/s

Table C-1. Glossary of Terms-Continued

Mnemonic	*Description*
RIOOKIMT	Symbol Rate Switch Selection Between 100 and 999.99 kb/s True
RI010OKT	Symbol Rate Switch Selection Between 19.2 and 99.999 kb/s
R15MIX	Synthesizer 15 MHz Input To Mixer
R45MA	Receive 45 MHz Amplifier Input
R45MIX	Synthesizer 45 MHz Input To Mixer
R45MVCO	Receive 45 MHz VCO Output
SGNTD	Sign Bit To Decoder
SGN-11	PN Sequence Generator External Jumper From Stage 11
SMPSTRC	External Jumper To Resync Comparator
SQGENCK	Sequence Generator Clock
SYNCNII	2047 Bit Sync
TBSBSSC	Frequency Control To Transmit Frequency Synthesizer VCO
TBSDATC	Transmit Bit Sync Data Complement Output
TBSDATT	Transmit Bit Sync Data True Output (Test)
TBSLOLC	Transmit Bit Sync Loss Of Lock
TBS2RC	Transmit Bit Sync Clock X2
TDAC-1 TDAC-2 TDAC-3 TDAC-4 TDAC-5 TDAC-6 TDAC-7 TDAC-8	Transmit Loop Filter Output To D/A Converter
TDUMP	Transmit Integrator Dump Signal
TESTM15	--15 V To Monitor Meter
TESTM5V	-5 V To Monitor Meter
TESTP15	+15 V To Monitor Meter
TESTP5V	+5 V To Monitor Meter
THERMO	Overtemperature indication
TLDPGM	Transmit Load Program
TMIXD	30 + MHz To Transmit Reference Divider
TMIXO	Transmit Synthesizer 30 - 10 MHz From Mixer/Output Amplifier
TSAMP	Transmit Sample From Programmable Divider
TSCMO	Stable Clock To Reference Divider
TSCTCXO	45 MHz To Stable Clock
TSC45M	15 MHz Reference To Transmit Stable Clock
TSEQ+	Test Sequence (2047 Bit PRN)
TSEQBRC	Test Sequence Bit Rate
TSTALT	Test Alternate Data
TSTICF	Test ICF Input
TSTRXBS	Test Receive Bit Sync
TSTSEQ	Test Sequence
TSTTXBS	Test Transmit Bit Sync
TSYNTST	Transmit Test Of VCO Control Voltage To Meter
TTXLO	Transmit Synthesizer 15 MHz TCXO Output
TVCO	Transmit 15 MHz VCO Output
TVCONT	Control To Transmit 15 MHz VCO
TXBSDTT	Data To Transmit Bit Sync
TXBSFL	Transmit Bit Sync Fault Indication
TXFAIL	Transmit Section Fault Indication
TXMXI	Transmit Rate Switch Setting Between 50000 and 99999
TXMX2	Transmit Rate Switch Setting Between 25000 and 49999
TXMX4	Transmit Rate Switch Setting Between 12500 and 24999
TXMX8	Transmit Rate Switch Setting Between 10000 and 12499
TXPDO-1 TXPDO-2 TXDPO-4 TXPDO-8	Digit 1 (Least Significant) Of Counter Encoder Program Output (Transmit Synthesizer)
TXPDI-1 TSPDI-2 TXPD1-4 TXPDI-8	Digit 2 Of Counter Encoder Program Output (Transmit Synthesizer)
TSPD2-1 TXPD2-2 TXPD)2-4 TXPD2-8	Digit 3 Of Counter Encoder Program Output (Transmit Synthesizer)

Table C-1. Glossary of Terms-Continued

Mnemonic	*Description*
TXPD3-1	Digit 4 Of Counter Encoder Program Output (Transmit
TXPD3-2	
TXPD3-4	Synthesizer)
TXPD3-8	
TXPD4-1	Digit 5 (Most Significant) Of Counter Encoder Program Output
TXPD4-2	
TXPD4-4	(Transmit Synthesizer)
TXPD4-8	
TXPD5-1	Counter Encoder Multiplier Code To Synthesizer (Transmit
TXPD5-2	
TXPD5-4	Synthesizer)
TXPD5-8	
TXSYNRC	Transmit Bit Sync Clock Complement
TXSYNRT	Transmit Bit Sync Clock True
TXSYNTR	Internal Clock Generator Output
TX9-0-1	Least Significant Transmit Rate Digit Includes 9's Complement Of 20
TX9-0-2	Least Significant Transmit Rate Digit Includes 9's Complement Of 2'
TX9-0-4	Least Significant Transmit Rate Digit Includes 9's Complement Of 2'
TX9-0-8	Least Significant Transmit Rate Digit Includes 9's Complement Of 2'
TX9-1-1	Nest Least Significant Transmit Rate Digit Includes 9's Complement Of 20
TX9-1-2	Next Least Significant Transmit Rate Digit Includes 9's Complement Of 21
TX9-1-4	Next Least Significant Transmit Rate Digit Includes 9's Complement Of 2'
TX9-1-8	Next Least Significant Transmit Rate Digit Includes 9's Complement Of 2'
TX9-2-1	Middle Significant Digit Transmit Rate Digit Includes 9's Complement Of 2o
TX9-2-2	Middle Significant Digit Transmit Rate Digit Includes 9's Complement Of 2'
TX9-2-4	Middle Significant Digit Transmit Rate Digit Includes 9's Complement Of 2'
TX9-2-8	Middle Significant Digit Transmit Rate Digit Includes 9's Complement Of 2'
TX9-3-1	Next Most Significant Transmit Rate Digit Includes 9's Complement Of 20
TX9-3-2	Next Most Significant Transmit Rate Digit Includes 9's Complement Of 21
TX9-3-4	Next Most Significant Transmit Rate Digit Includes 9's Complement Of 2'
TX9-3-8	Next Most Significant Transmit Rate Digit Includes 9's Complement Of 2'
TX9-4-1	Most Significant Transmit Rate Digit Includes 9's Complement Of 2'
TX9-4-2	Most Significant Transmit Rate Digit Includes 9's Complement Of 2'
TX9-4-4	Most Significant Transmit Rate Digit Includes 9's Complement Of 2'
TX9-4-8	Most Significant Transmit Rate Digit Includes 9's Complement Of 2'
TO-COM	+5 V To Transmit Data Rate Switch S5
T1-COM	+5 V To Transmit Data Rate Switch S4
T2-COM	+5 V To Transmit Data Rate Switch S3
T3-COM	+5 V To Transmit Data Rate Switch S2
T4-COM	+5 V To Transmit Data Rate Switch S1
TI-1OM	Transmit Rate Switch Selection Between 1 and 9.9999 Mb/s Complement
TI-1OMT	Transmit Rate Switch Selection Between 1 and 9.9999 Mb/s True
T10-100K	Transmit Rate Switch Selection Between 19.2 and 99.999 kb/s
T10OK-1M	Transmit Data Rate Switch Selection 100 and 999.99 kb/s
T100K1MT	Transmit Rate Switch Selection Between 100 and 999.99 kb/s True
T10100KT	Transmit Rate Switch Selection Between 19.2 and 99.999 kb/s True
T45MA	Transmit 45 MHz Amplifier Input
T45MIX	45 MHz Input To Mixer
T45MVCO	Transmit 45 MHz VCO Output
2RCKFE	2X Clock To Coder
2RCKFEC	2R Clock From Encoder
2RCKTD	2R Clock To Decoder
2RCKTE	2R Clock To Encoder Complement

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ARNO & USAR: None.

For explanation of abbreviations used, e AR 10-bO0.

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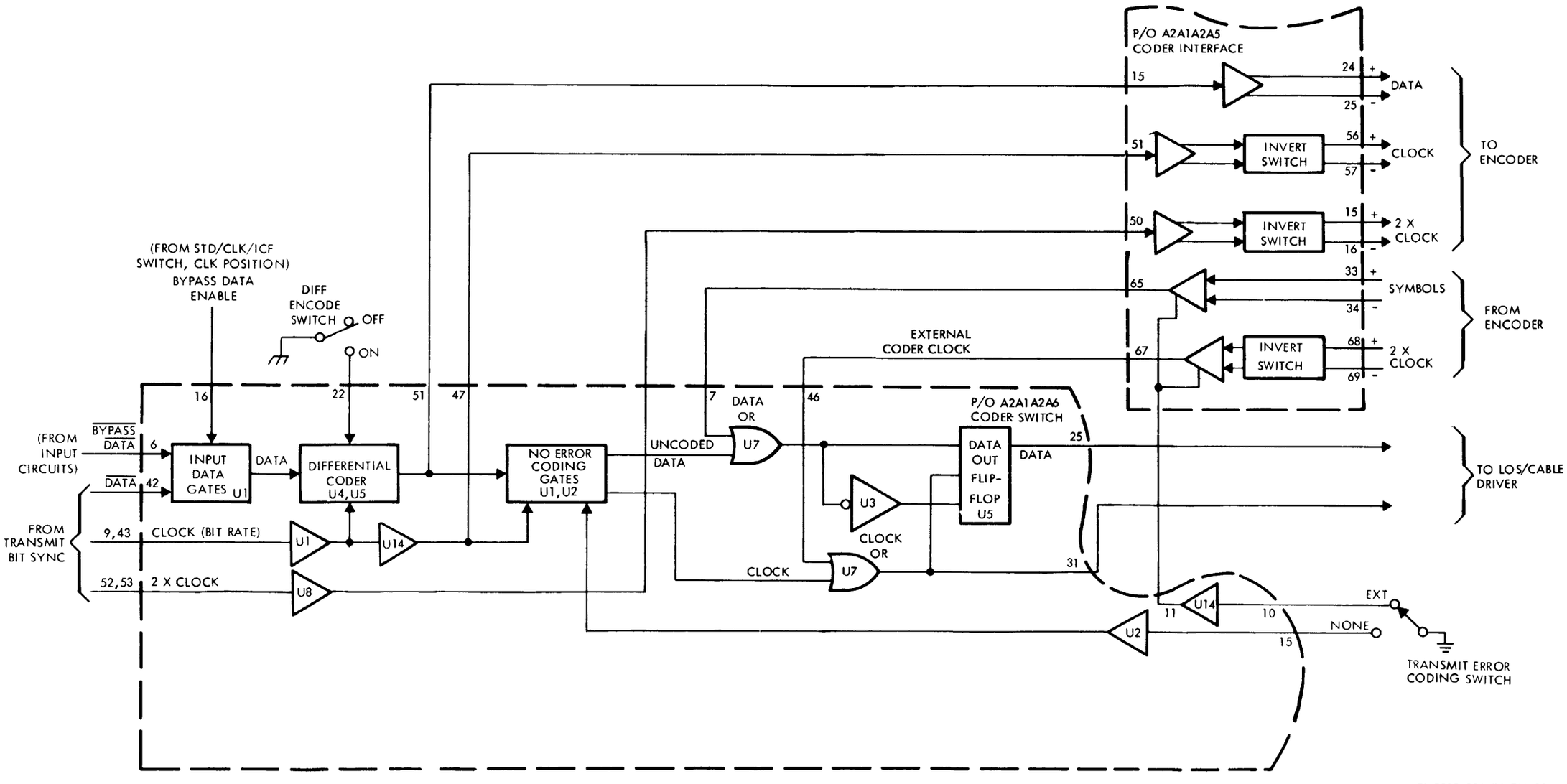

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Figure FO-1. Coders and interface, functional block diagram.

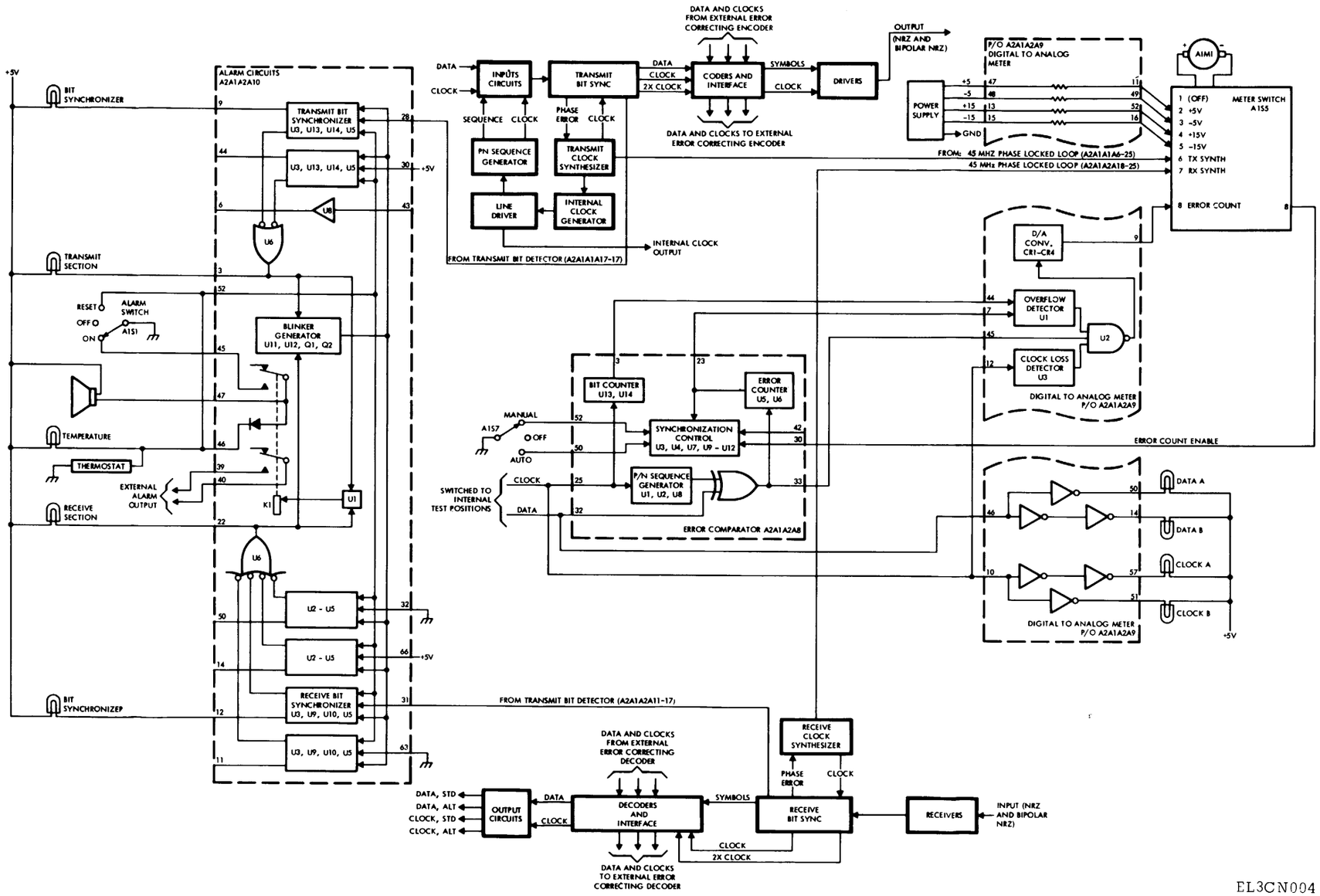


Figure FO-2. Fault and status monitor, functional block diagram.

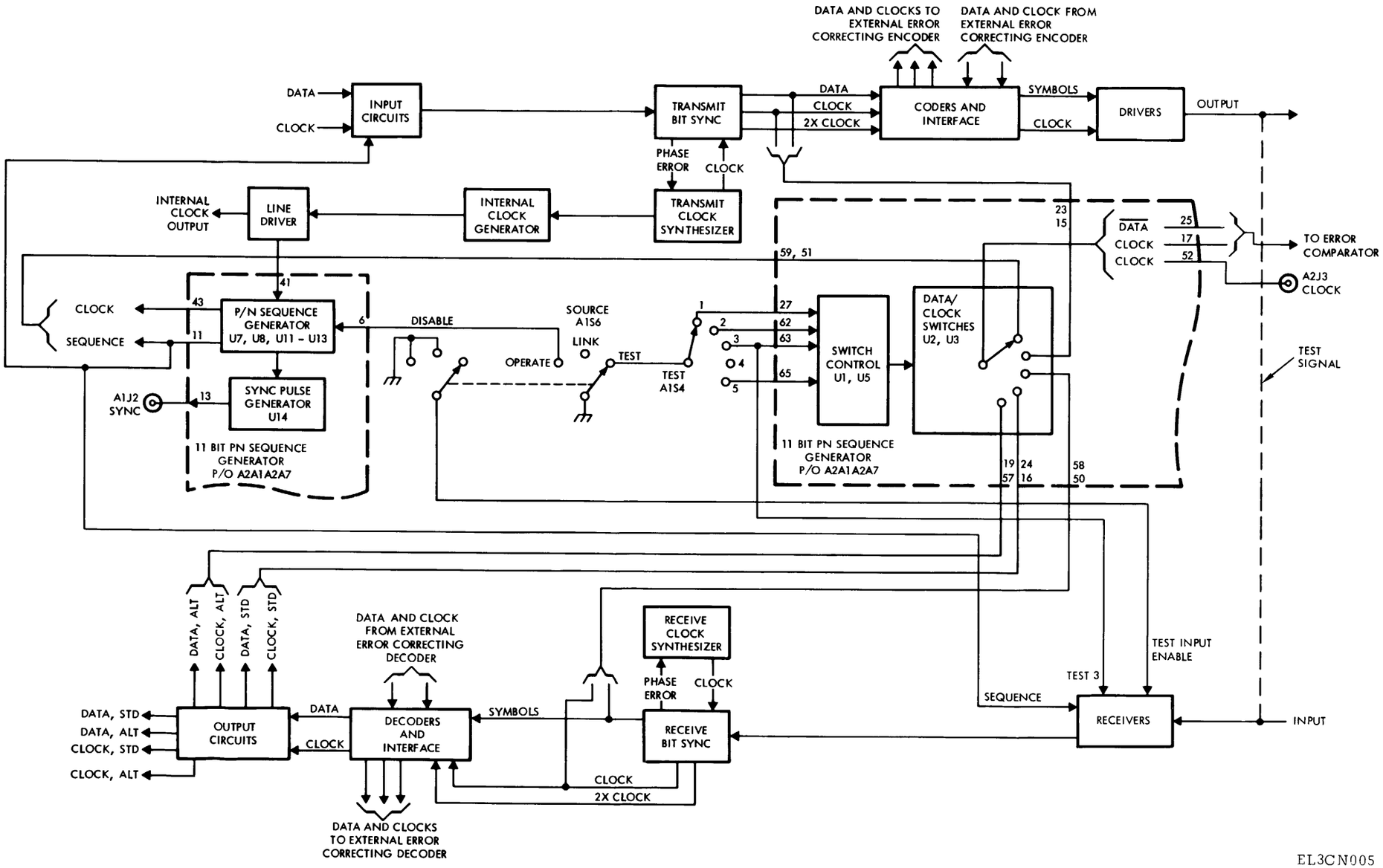


Figure FO-3. Test circuits, functional block diagram.

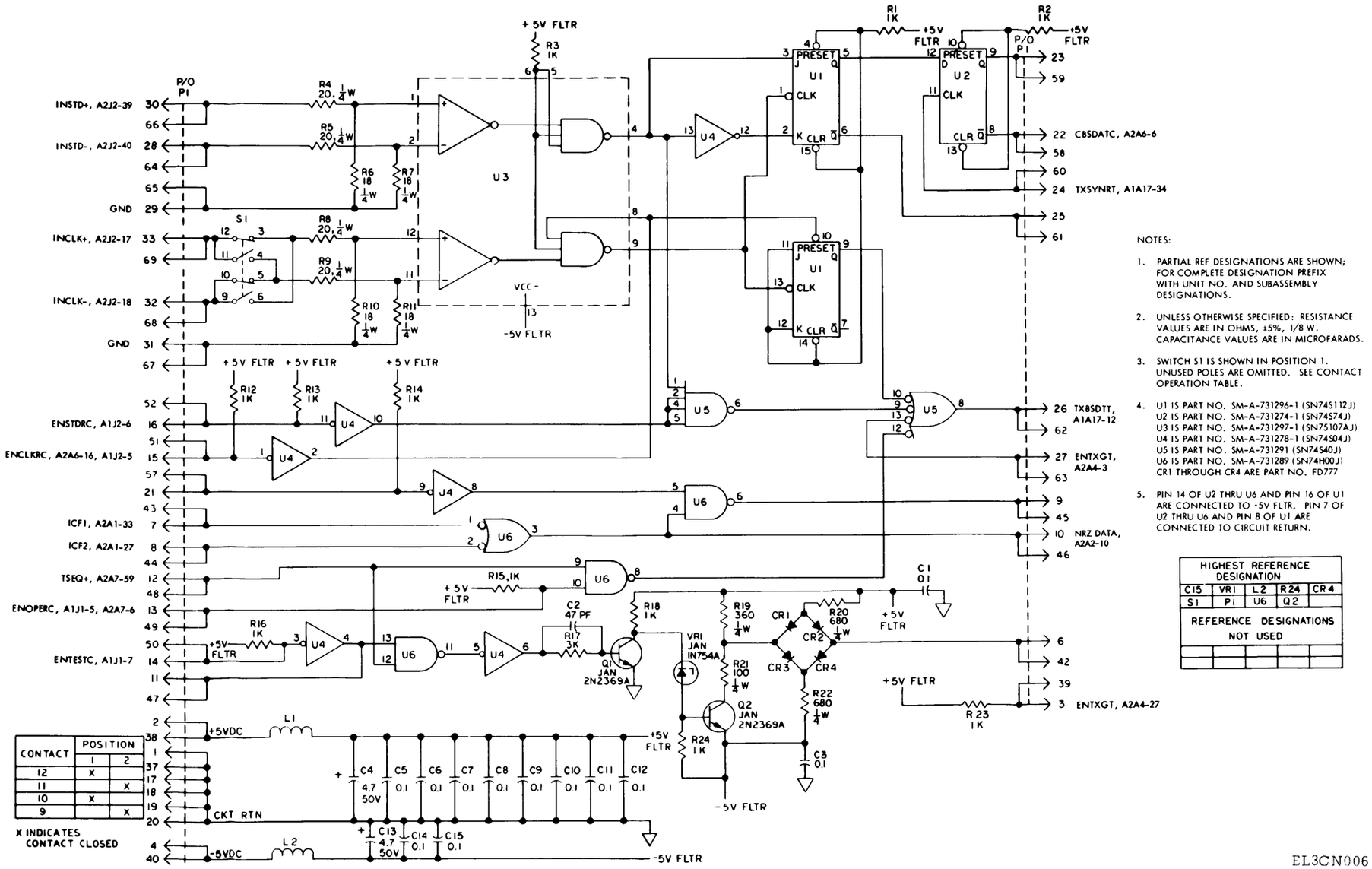
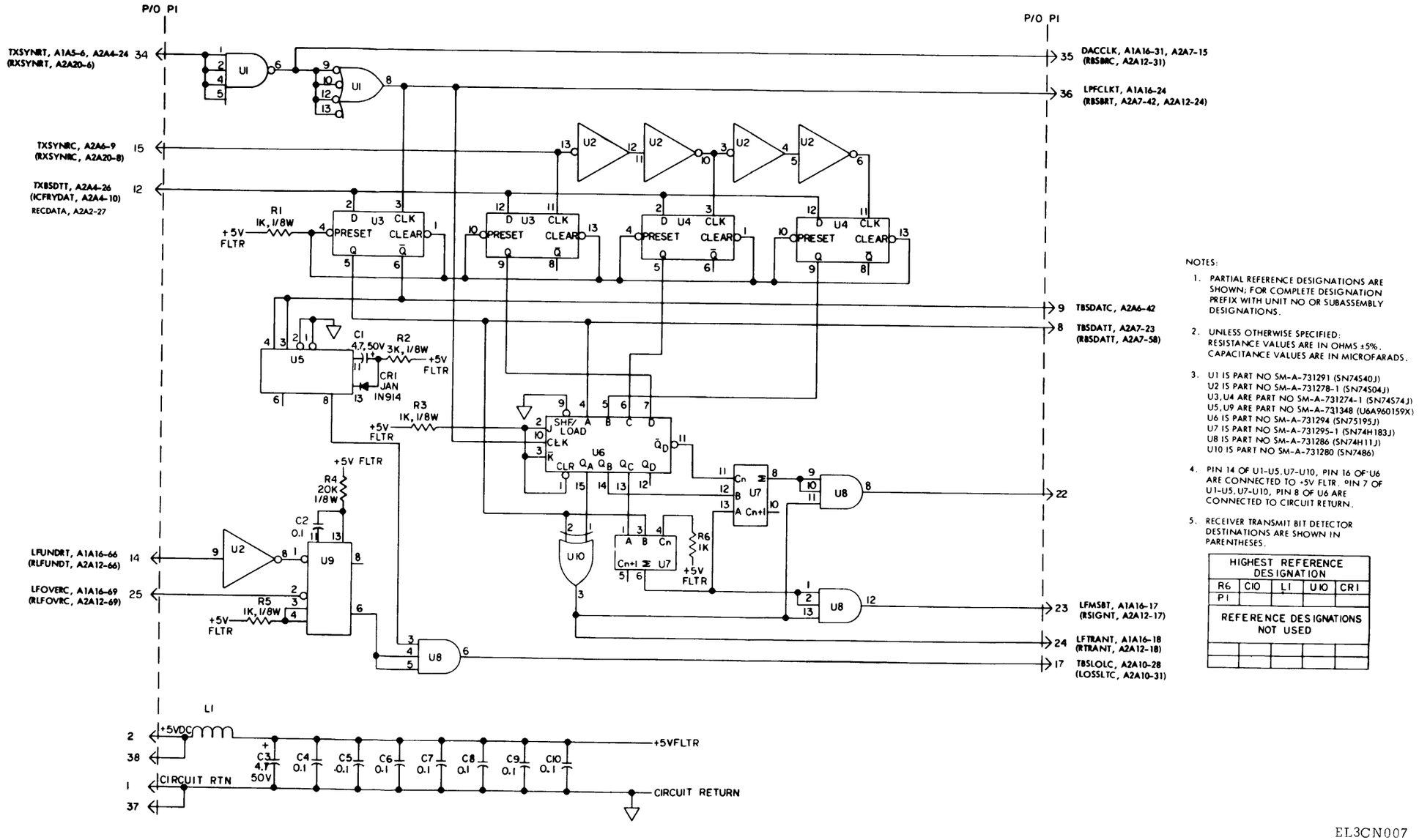


Figure FO-4. Input interface, A2A1A2A4 (SM-D-742037) schematic diagram.



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO OR SUBASSEMBLY DESIGNATIONS.
2. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS ±5%. CAPACITANCE VALUES ARE IN MICROFARADS.
3. U1 IS PART NO SM-A-731291 (SN74S40J)
   U2 IS PART NO SM-A-731278-1 (SN74S04J)
   U3, U4 ARE PART NO SM-A-731274-1 (SN74S74J)
   U5, U9 ARE PART NO SM-A-731348 (U6A960159X)
   U6 IS PART NO SM-A-731294 (SN75195J)
   U7 IS PART NO SM-A-731295-1 (SN74H183J)
   U8 IS PART NO SM-A-731286 (SN74H11J)
   U10 IS PART NO SM-A-731280 (SN7486)
4. PIN 14 OF U1-U5, U7-U10, PIN 16 OF U6 ARE CONNECTED TO +5V FLTR. PIN 7 OF U1-U5, U7-U10, PIN 8 OF U6 ARE CONNECTED TO CIRCUIT RETURN.
5. RECEIVER TRANSMIT BIT DETECTOR DESTINATIONS ARE SHOWN IN PARENTHESES.

HIGHEST REFERENCE DESIGNATION				
R6	C10	L1	U10	CR1
P1				
REFERENCE DESIGNATIONS NOT USED				

EL3CN007

Figure FO-5. Transmit bit detector, A2A1A1A17, A2A1A2A11 (SM-D-742045) schematic diagram.

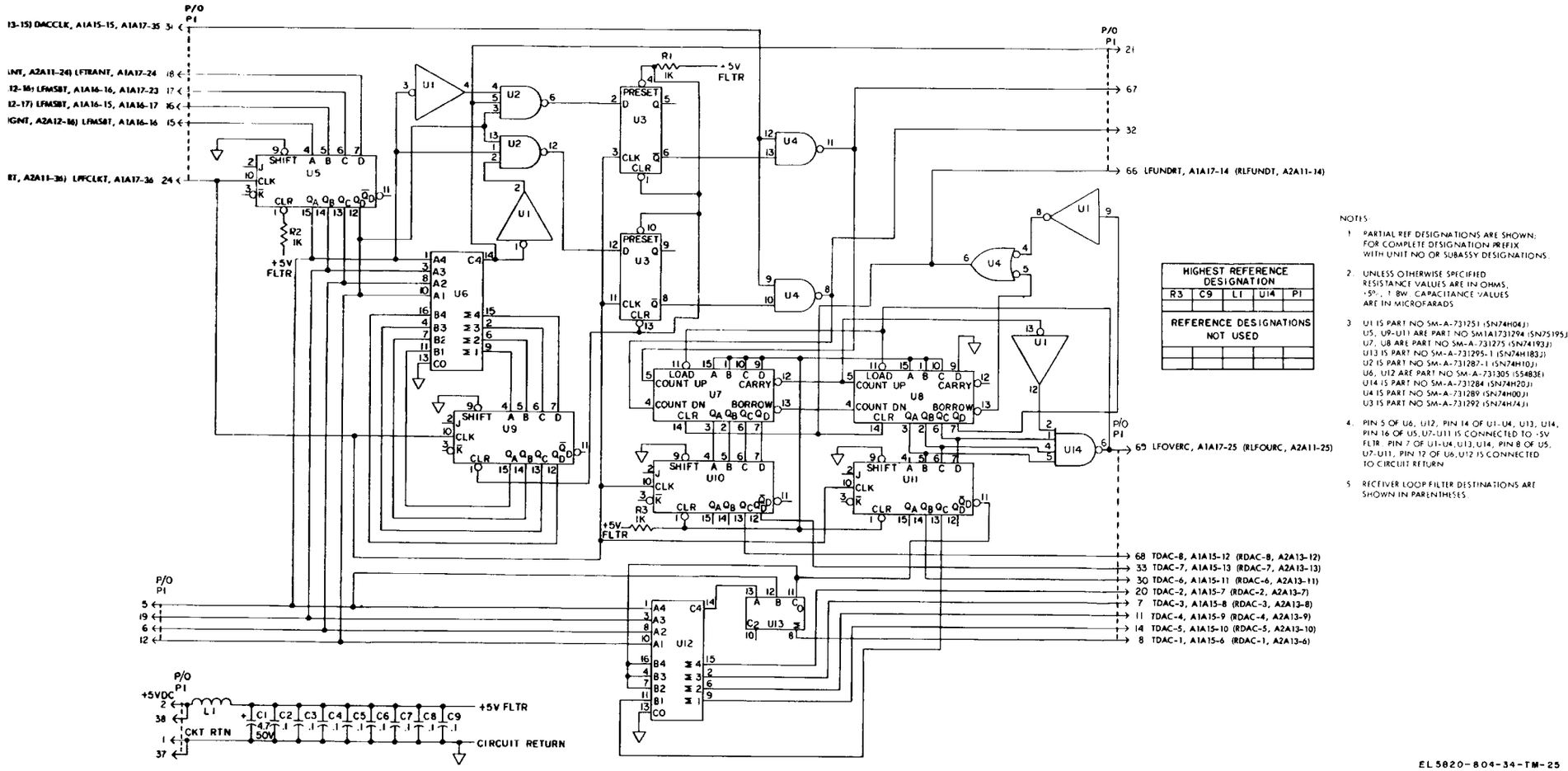


Figure FO-6. Loop filter, A2A1A1A16, A2A1A2A12 (SM-D-731221) schematic diagram.

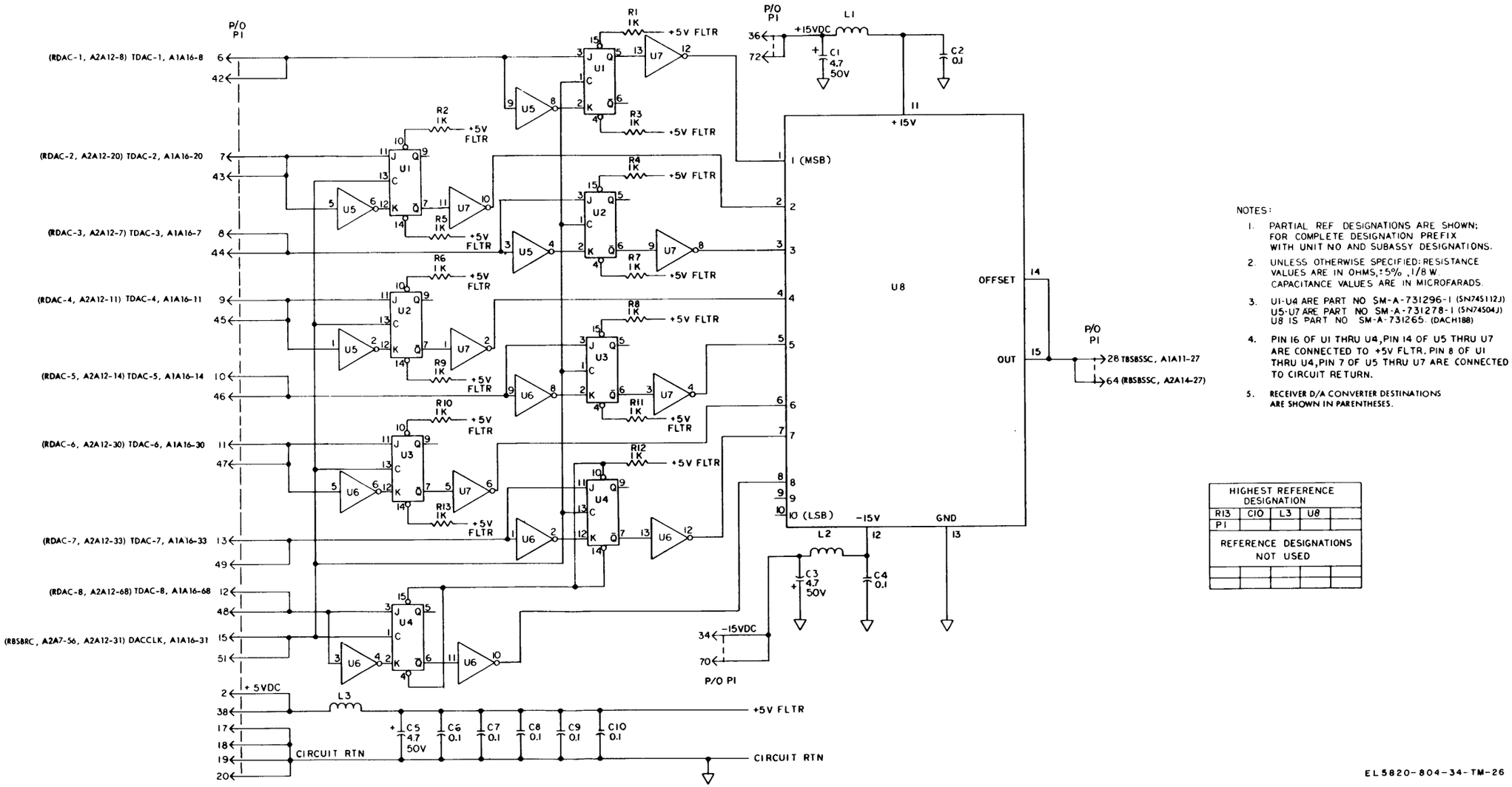


Figure FO-7. Digital-to-analog converter, A2A1A1A15, A2A1A2A13 (SM-D-731217) schematic diagram.

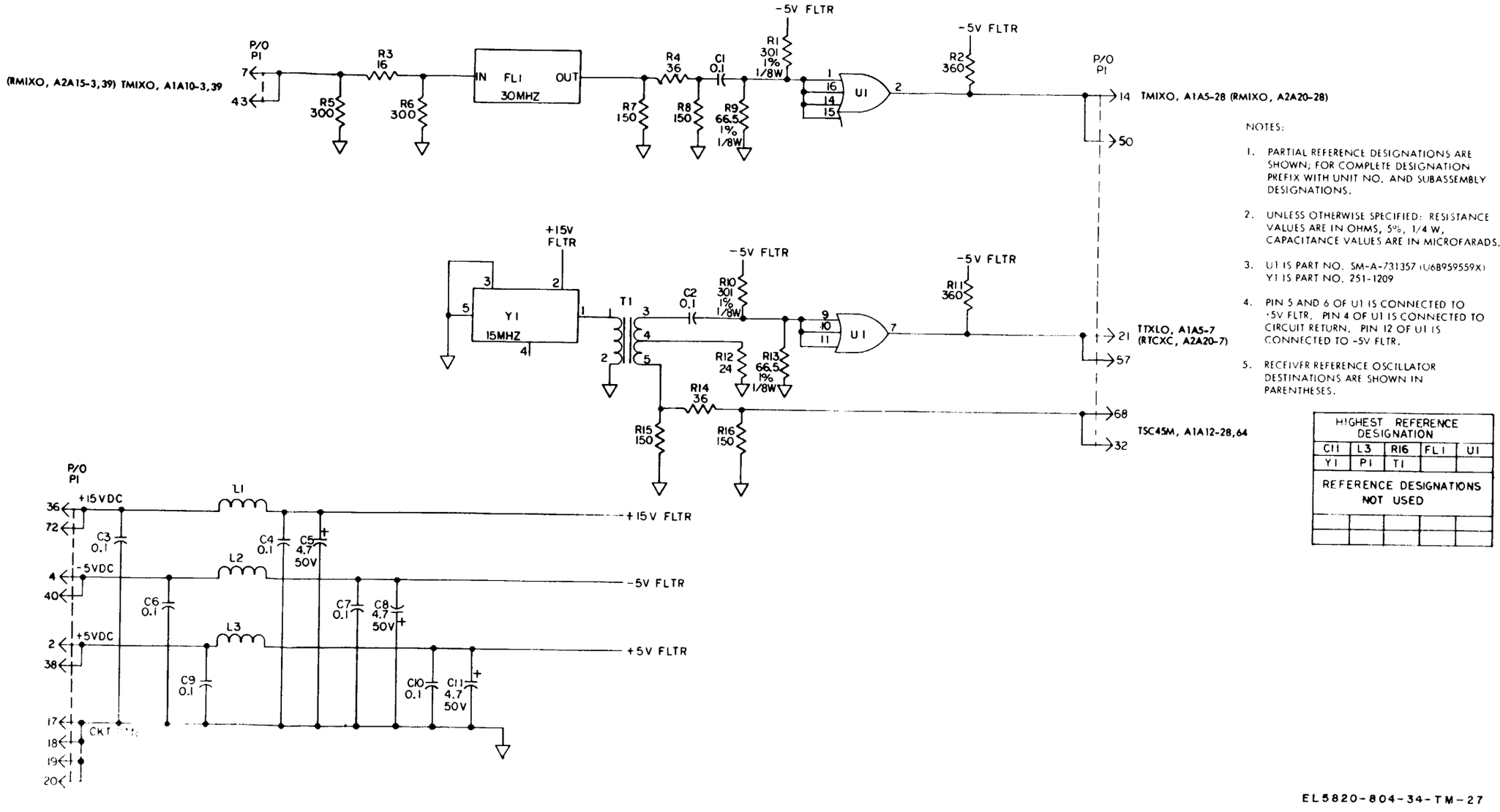


Figure FO-8. Reference oscillator, A2A1A1A3, A2A1A2A21 (SM-D-742129) schematic diagram.

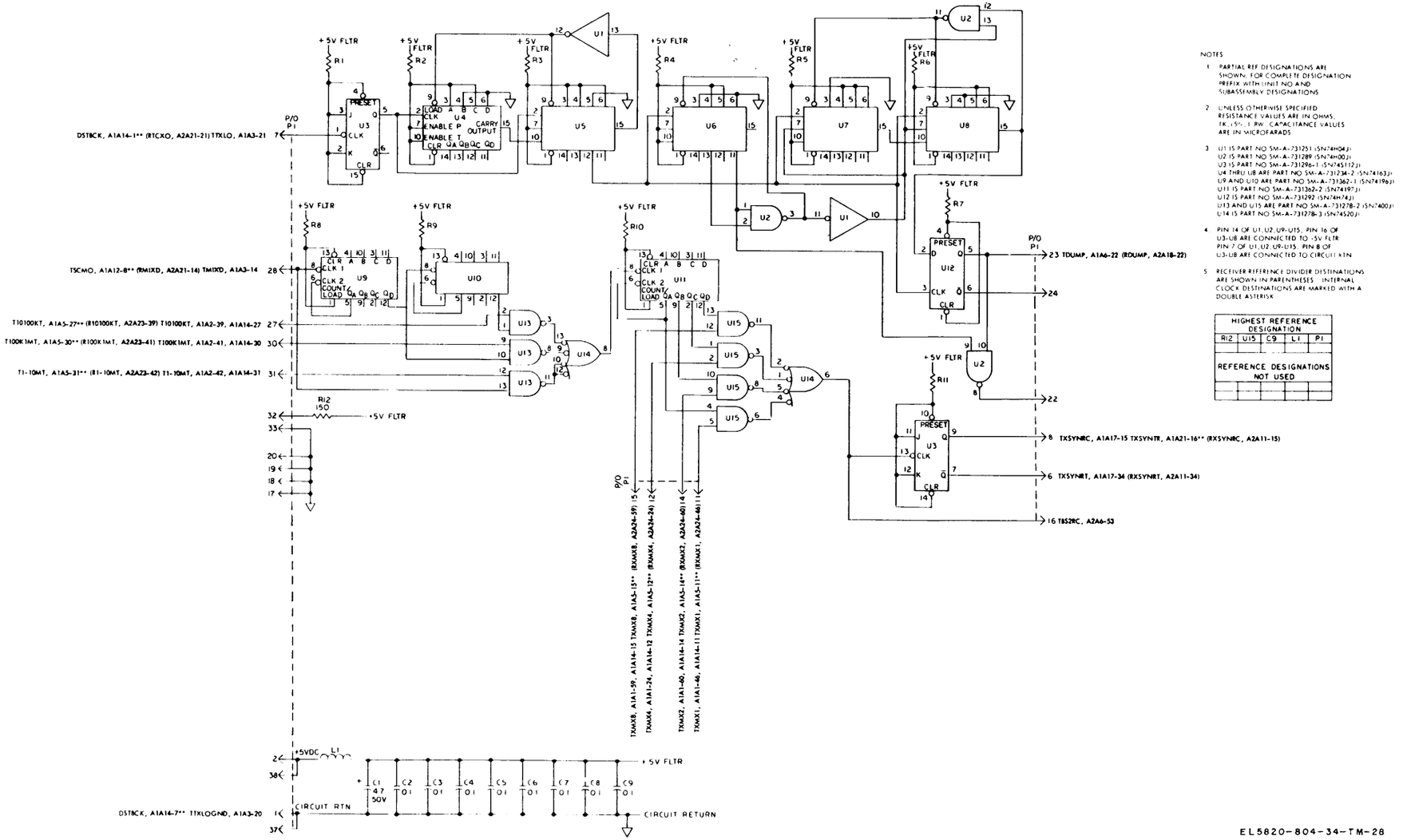


Figure FO-9. Reference divider, A2A1A1A5, A2A1A2A20 (SM-D-742133), schematic diagram.

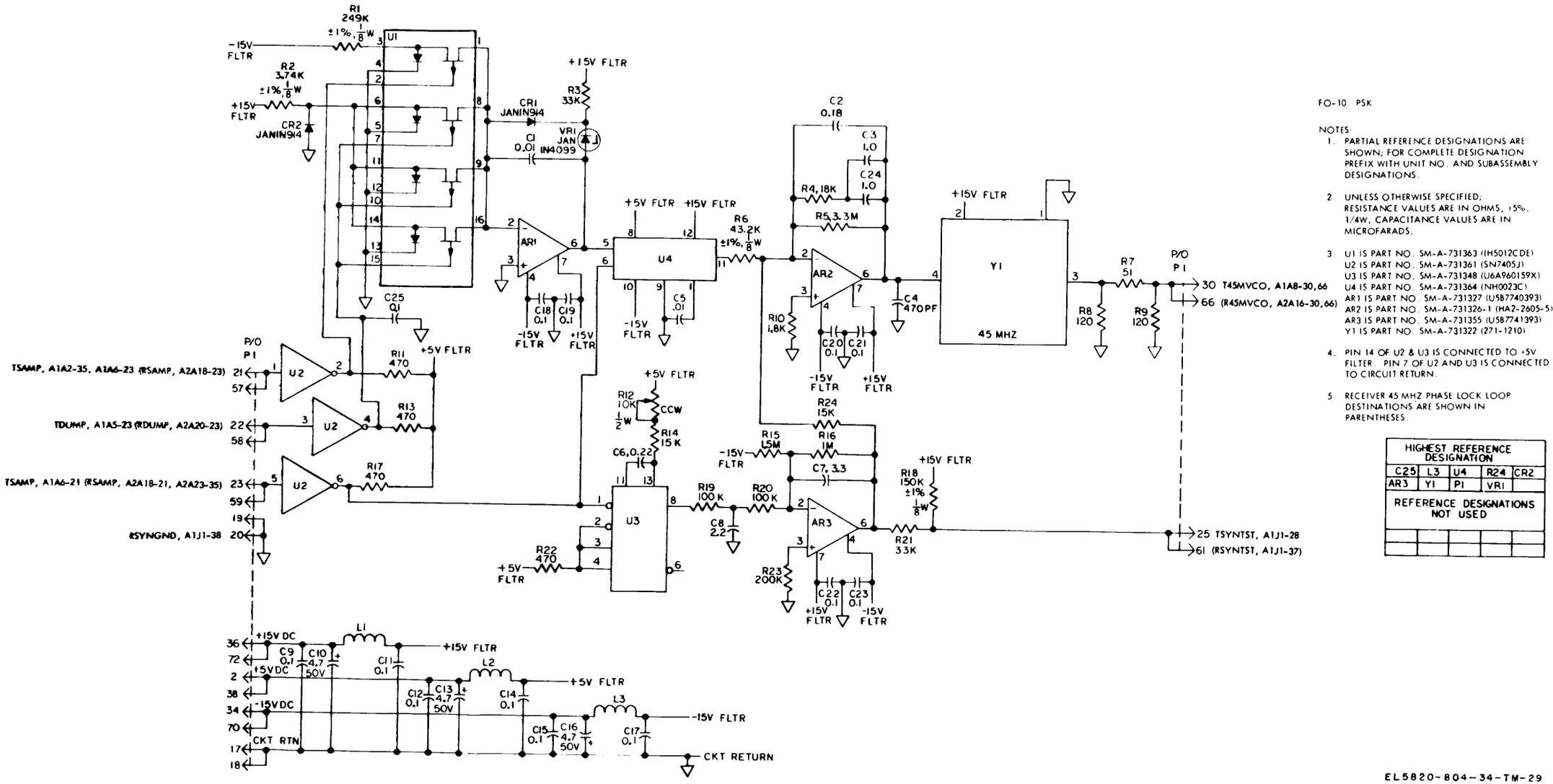


Figure FO-10. 45 MHz phase lock loop, A2A1A1A6, A2A1A2A18 (SM-D-742113) schematic diagram.

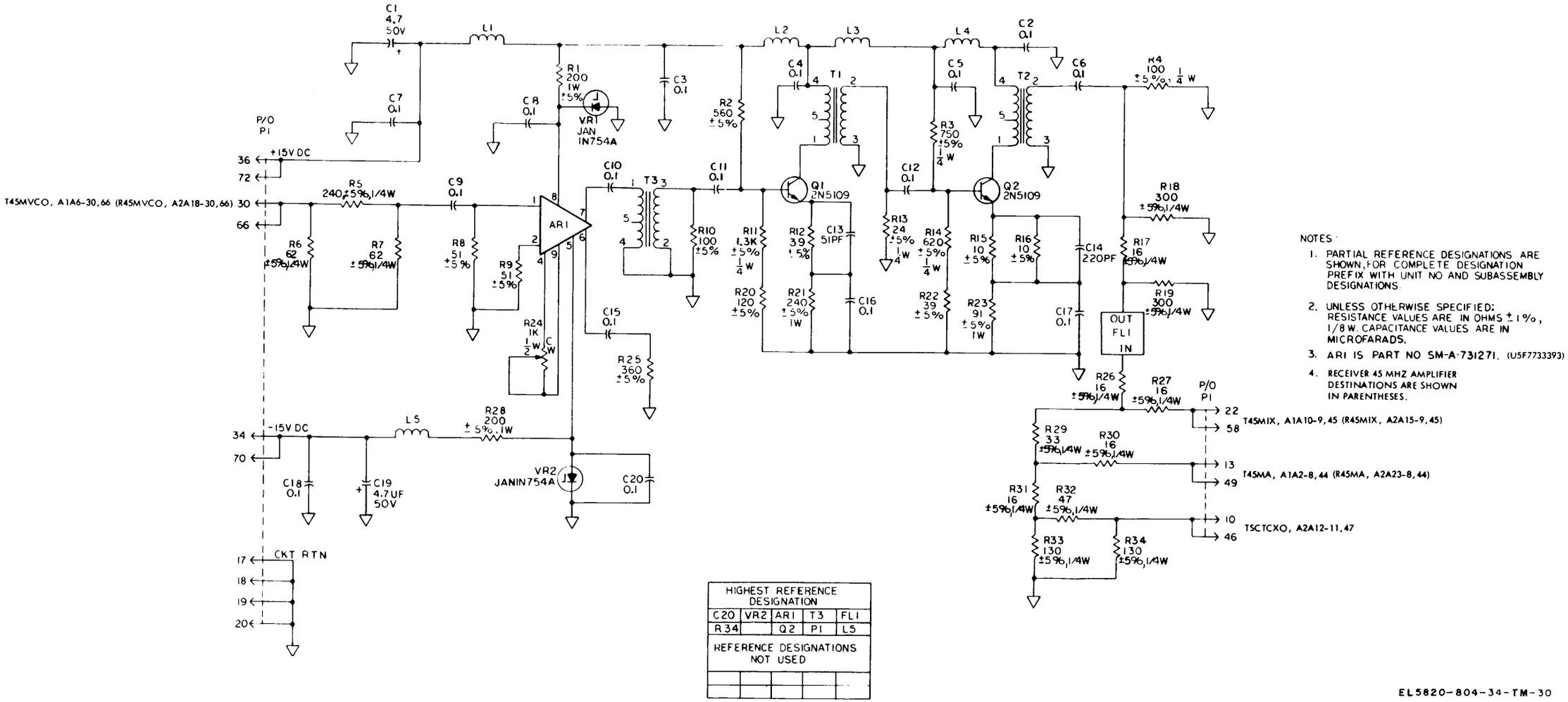


Figure FO-11. 45 MHz amplifier, A2A1A1A8, A2A1A2A16 (SM-D-742117) schematic diagram.

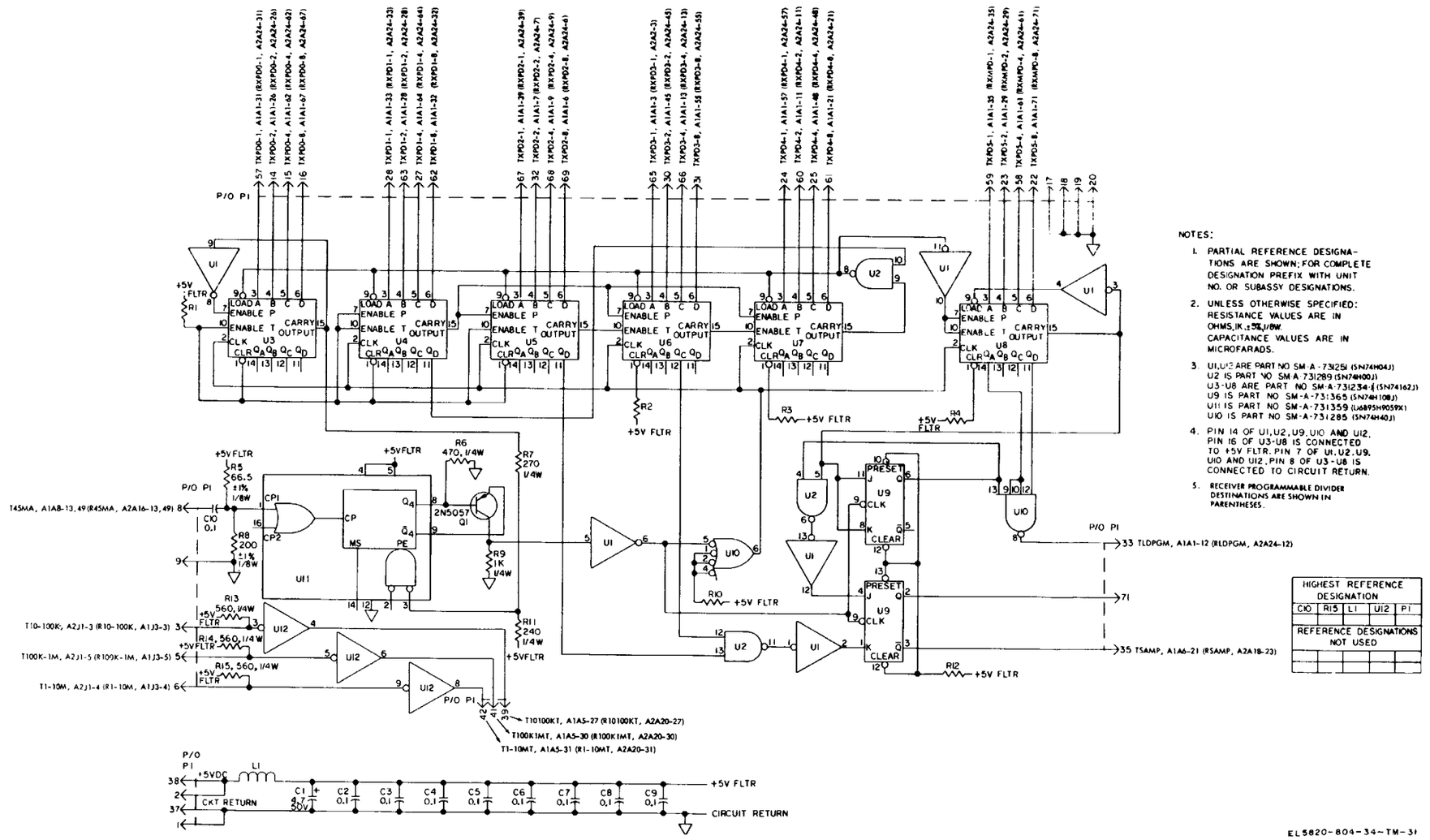


Figure FO-12. Programmable divider, A2A1A1A2, A2A1A2A23 (SM-D-742109) schematic diagram.

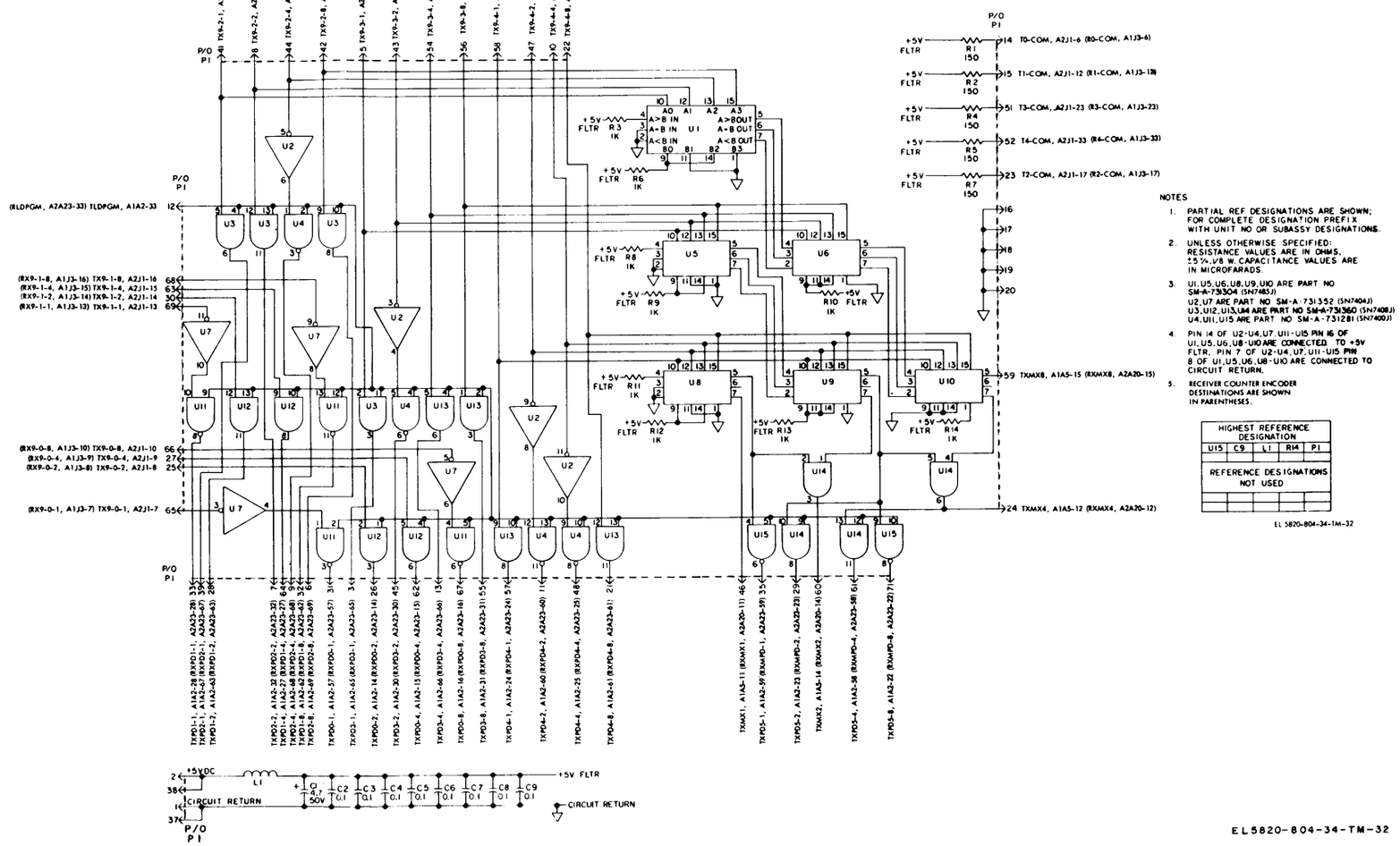
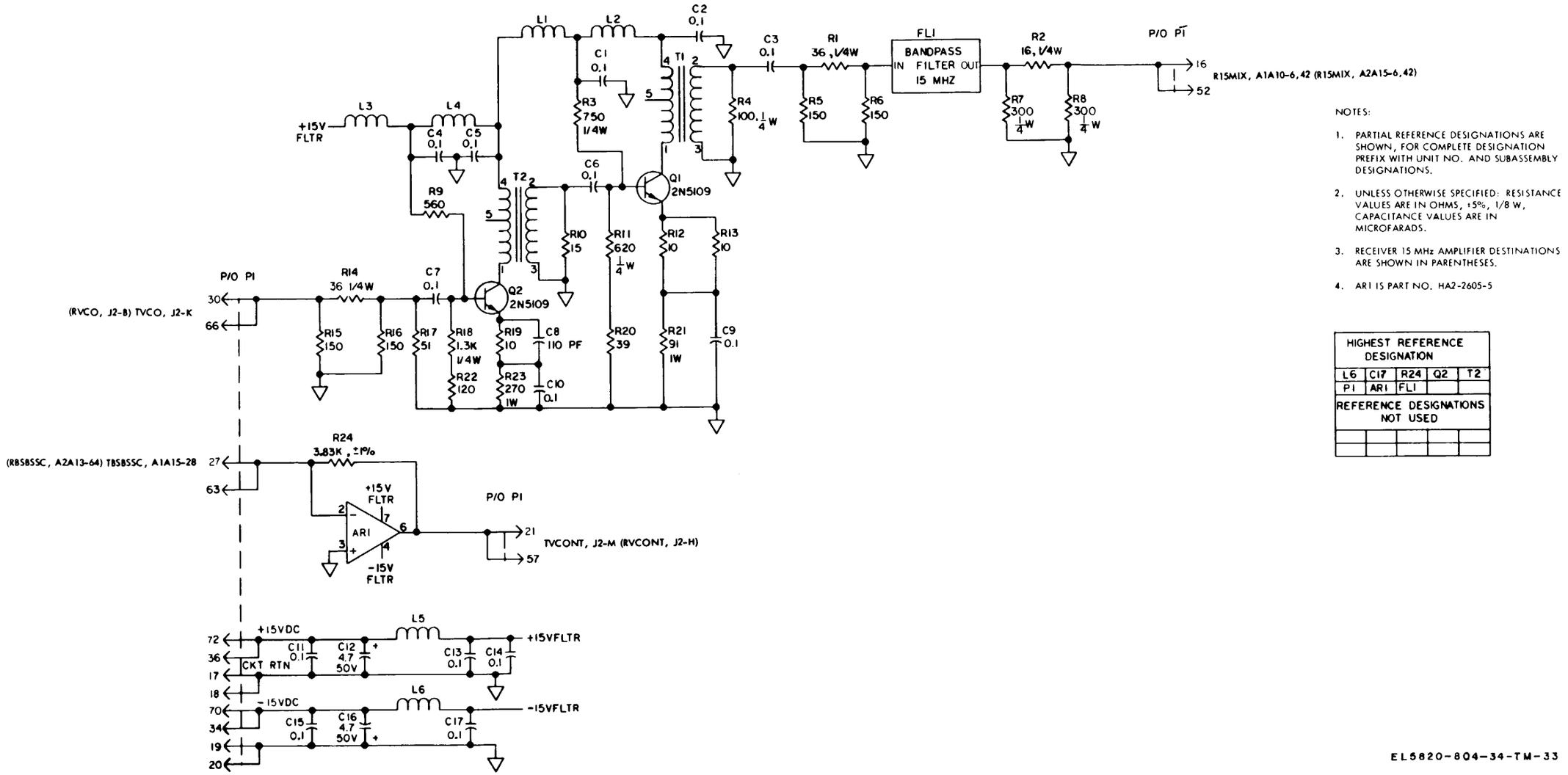


Figure FO-13. Counter encoder, A2A1A1A1, A2A1A2A24 (SM-D-742105) schematic diagram.



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. AND SUBASSEMBLY DESIGNATIONS.
2. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, ±5%, 1/8 W, CAPACITANCE VALUES ARE IN MICROFARADS.
3. RECEIVER 15 MHz AMPLIFIER DESTINATIONS ARE SHOWN IN PARENTHESES.
4. AR1 IS PART NO. HA2-2605-5

HIGHEST REFERENCE DESIGNATION				
L6	C17	R24	Q2	T2
P1	AR1	FL1		
REFERENCE DESIGNATIONS NOT USED				

EL5820-804-34-TM-33

Figure FO-14. 15 MHz amplifier, A2A1A1A1A11, A2A1A2A14 (SM-D-742121) schematic diagram.

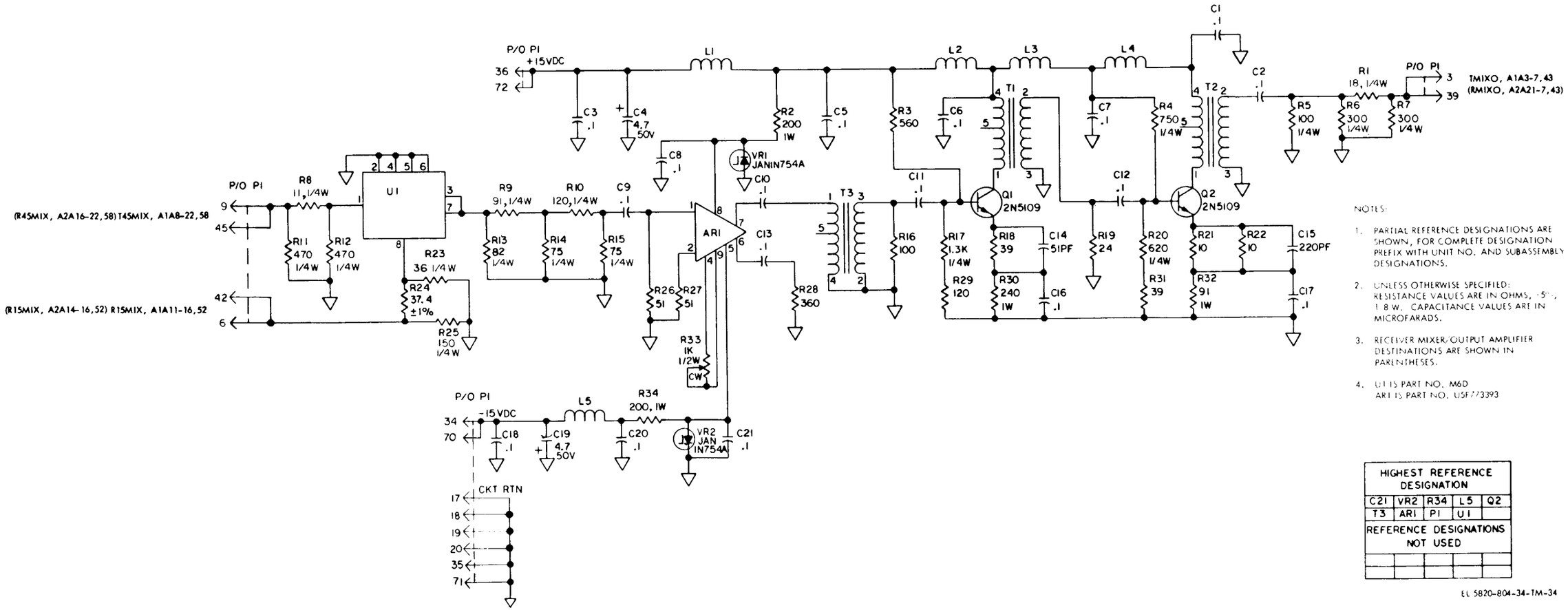


Figure FO-15. Mixer/output amplifier, A2A1A1A10, A2A1A2A15 (SM-D-742125) schematic diagram.

TM 11-5820-804-34

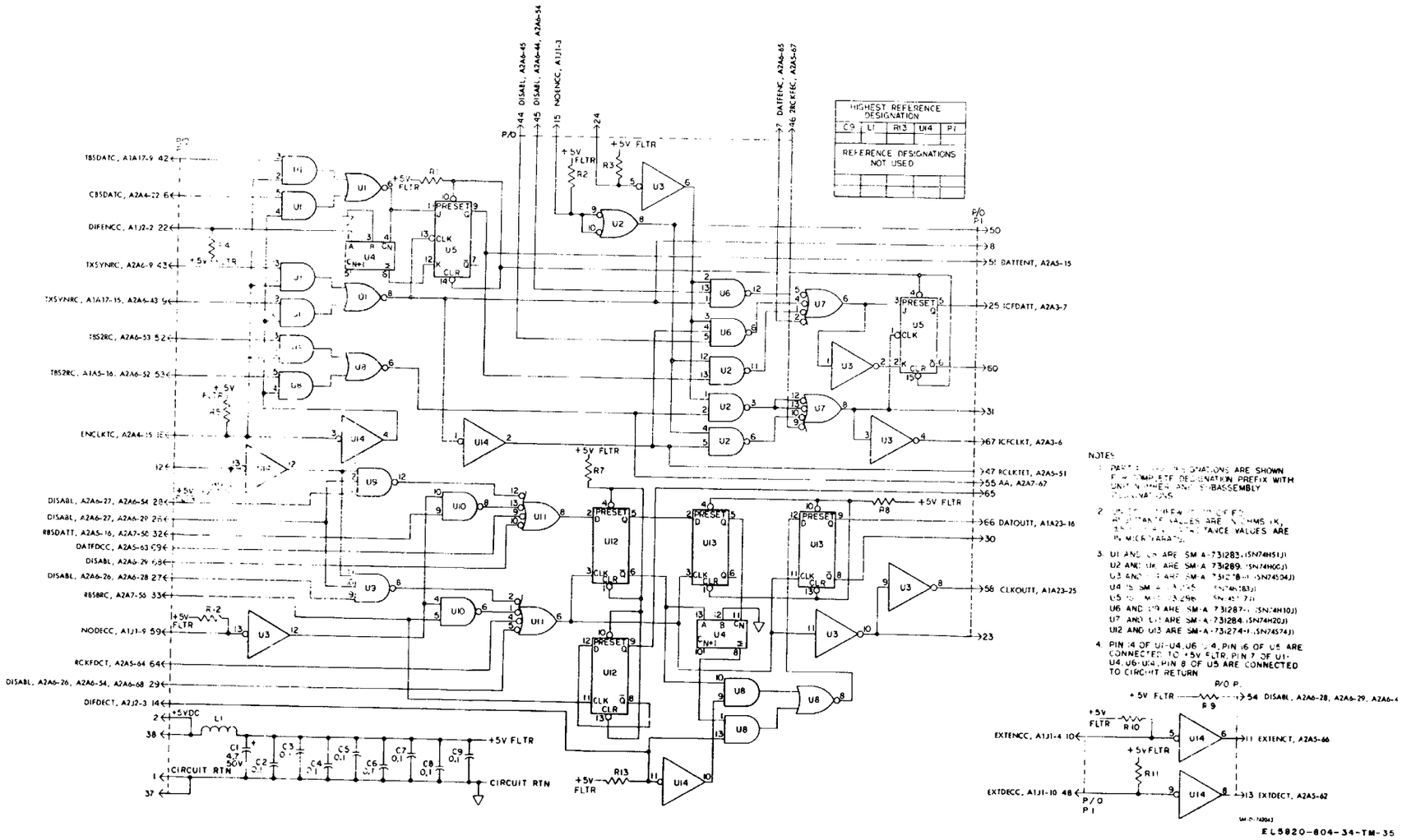


Figure FO-16. Coder switch, A2A1A2A6 (SM-D-742041) schematic diagram.

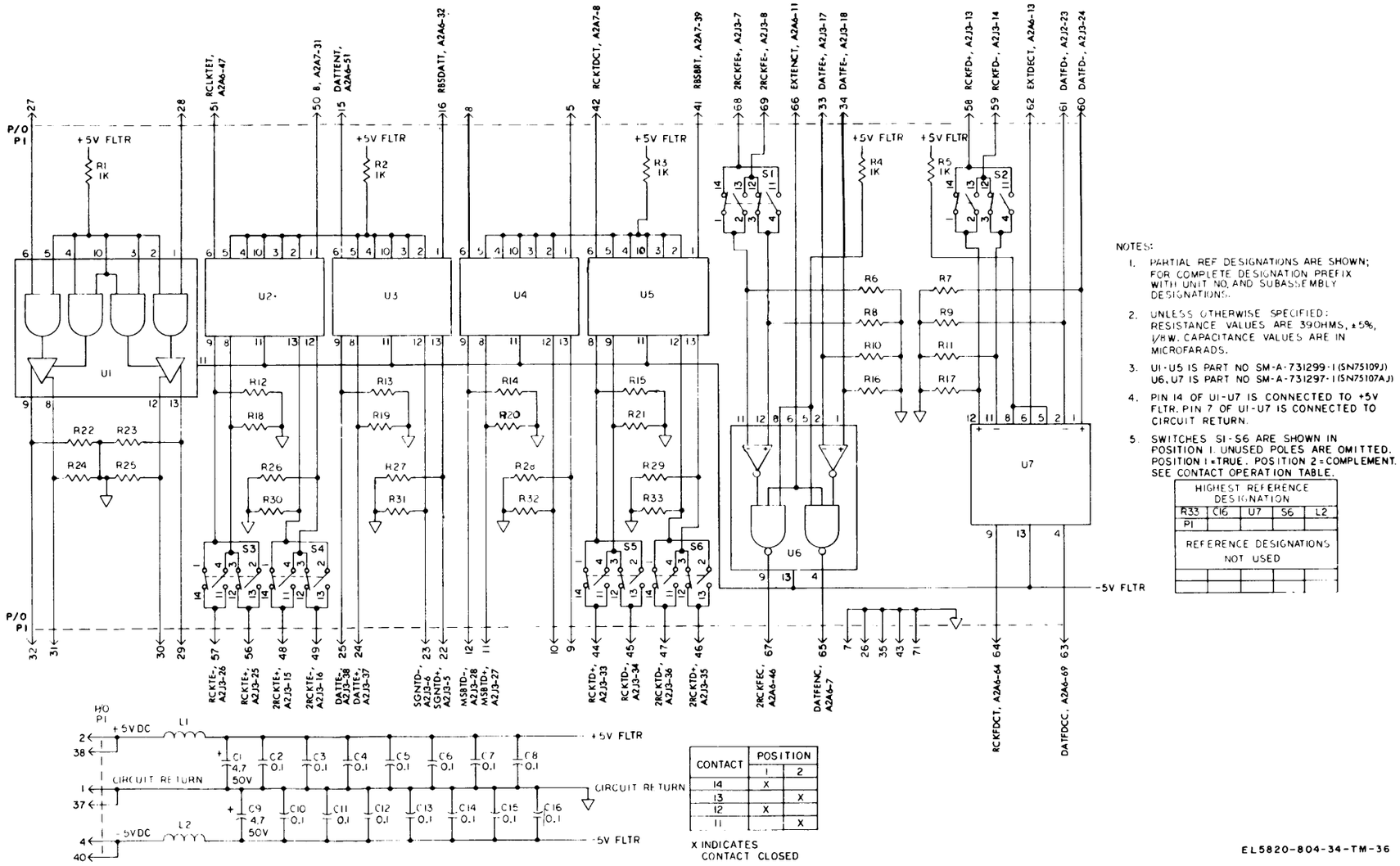


Figure FO-17. Coder interface, A2A1A2A6 (SM-D-742049) schematic diagram.

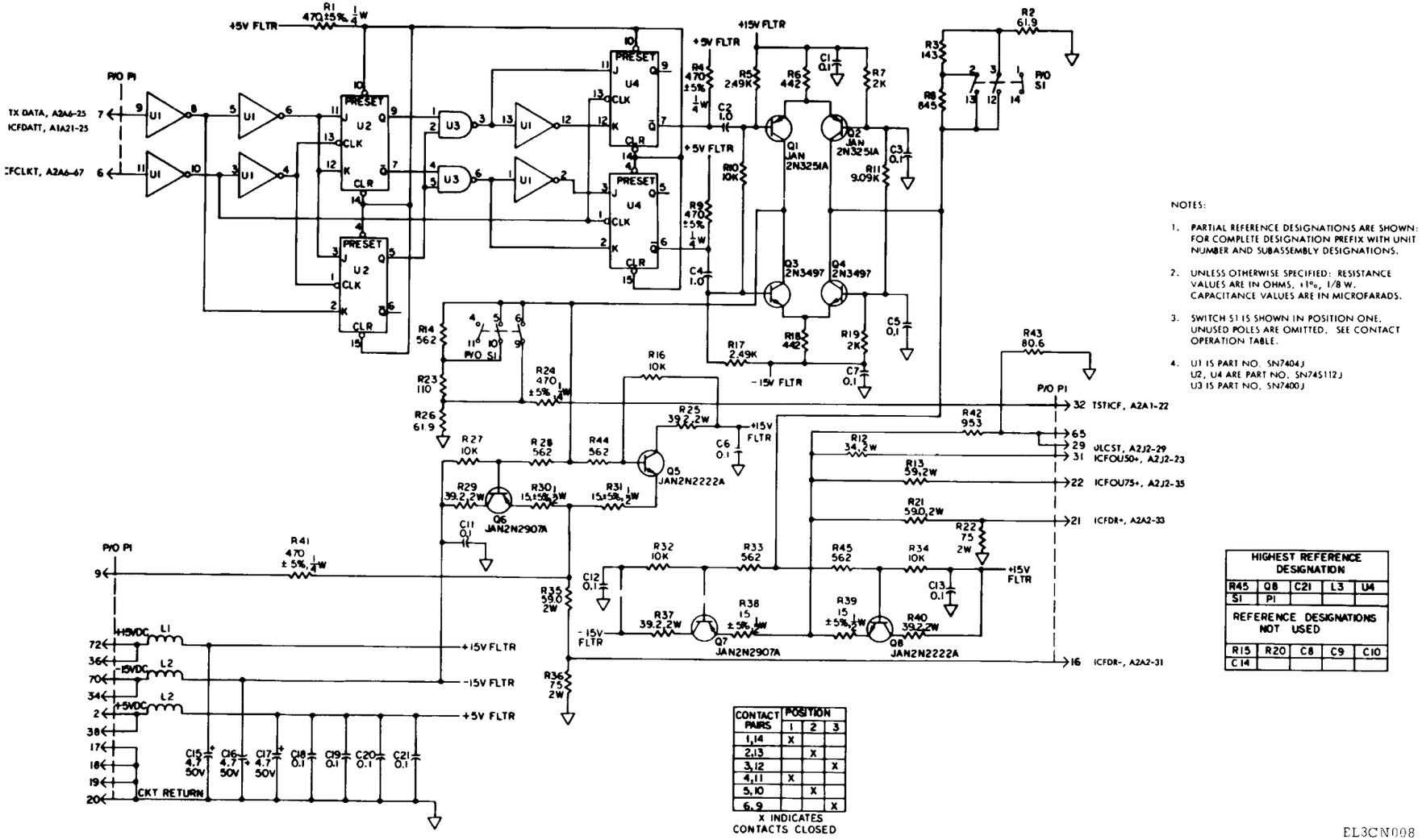
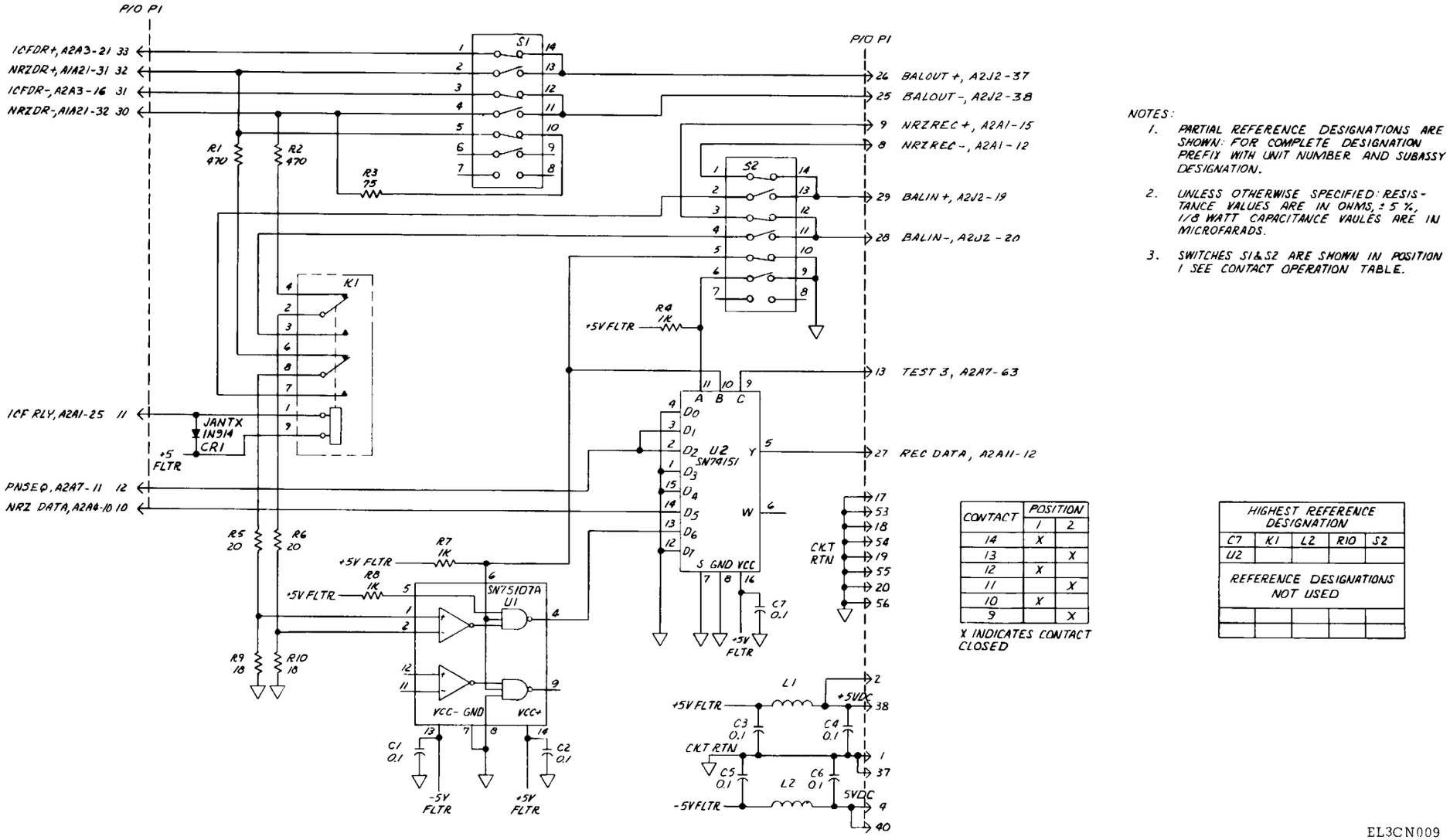


Figure FO-18. LOS/cable driver, A2A1A2A3 (SM-D-742081) schematic diagram.



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSY DESIGNATION.
2. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, ± 5 %, 1/8 WATT CAPACITANCE VAULES ARE IN MICROFARADS.
3. SWITCHES S1&S2 ARE SHOWN IN POSITION 1 SEE CONTACT OPERATION TABLE.

CONTACT	POSITION 1	POSITION 2
14	X	
13		X
12	X	
11		X
10	X	
9		X

X INDICATES CONTACT CLOSED

HIGHEST REFERENCE DESIGNATION				
C7	K1	L2	R10	S2
U2				
REFERENCE DESIGNATIONS NOT USED				

EL3CN009

Figure FO-18.1. NRZ interface, A2A1A2A2 (SM-D-877791) schematic diagram.

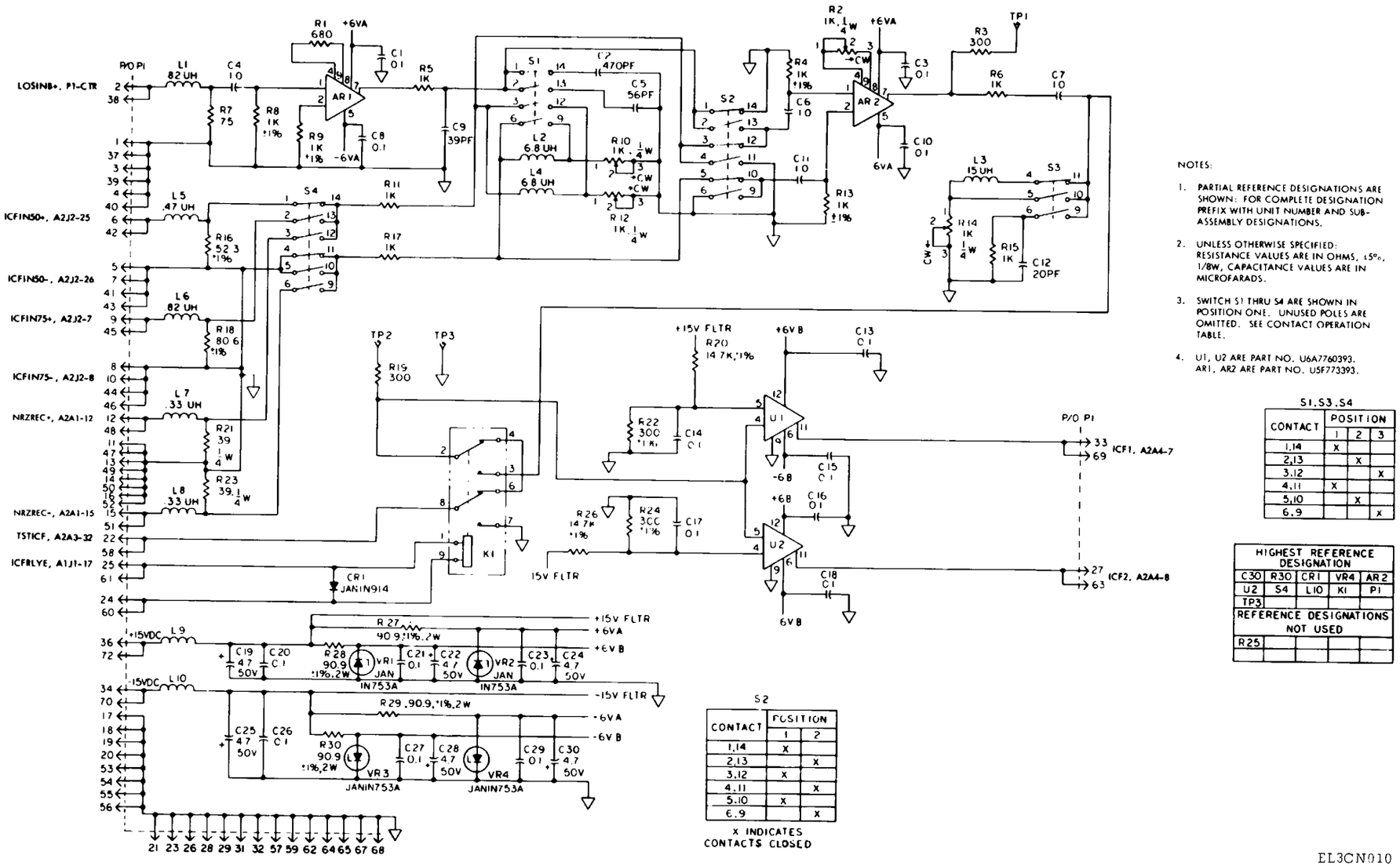


Figure FO-19. LOS/cable receiver and decoder. A2A1A2A1 (SM-D-742089) schematic diagram.

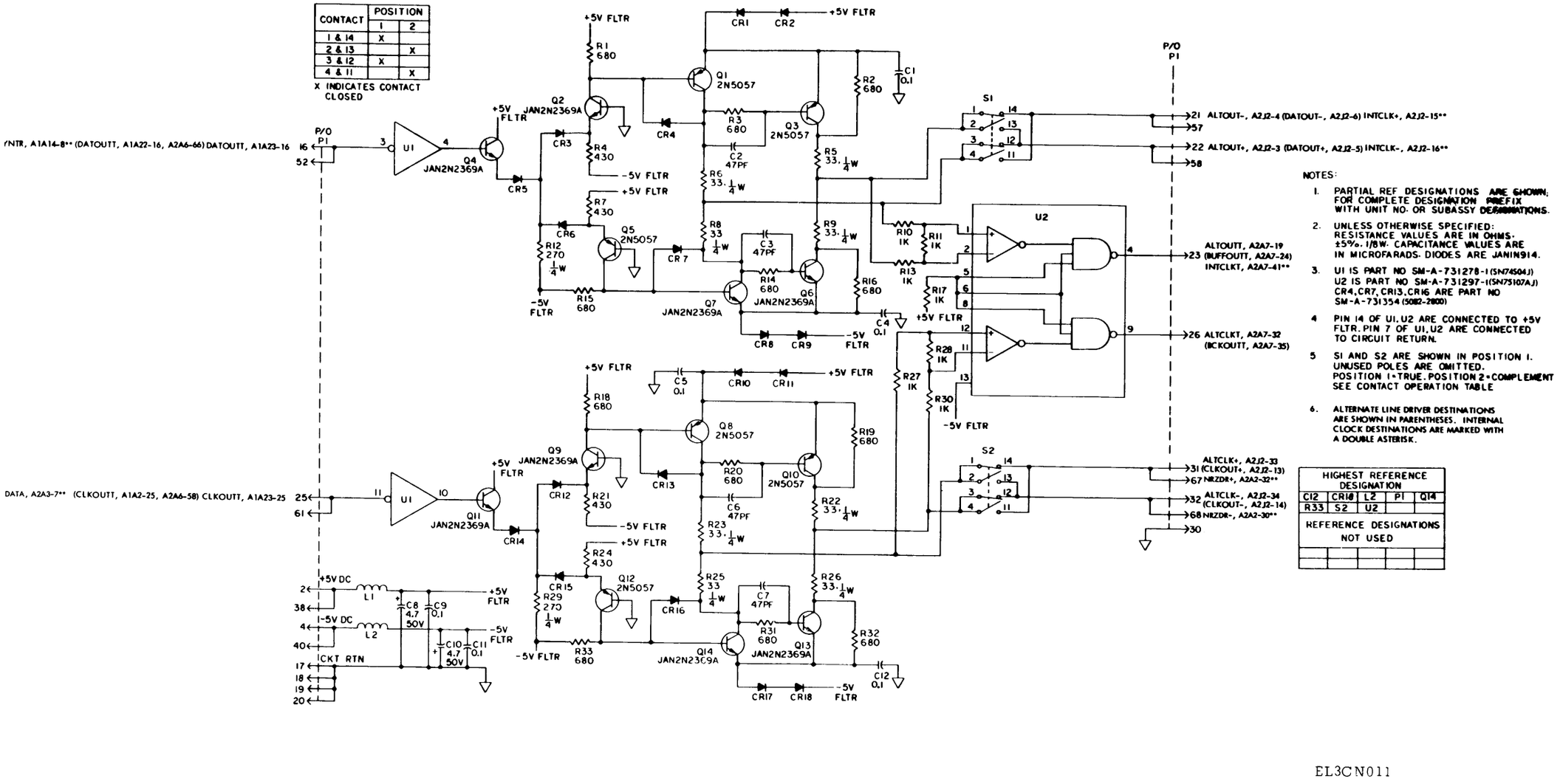


Figure FO-20. Line driver, A2A1A1A21, A2A1A1A22, A2A1A1A23 (SM-D-742053) schematic diagram.

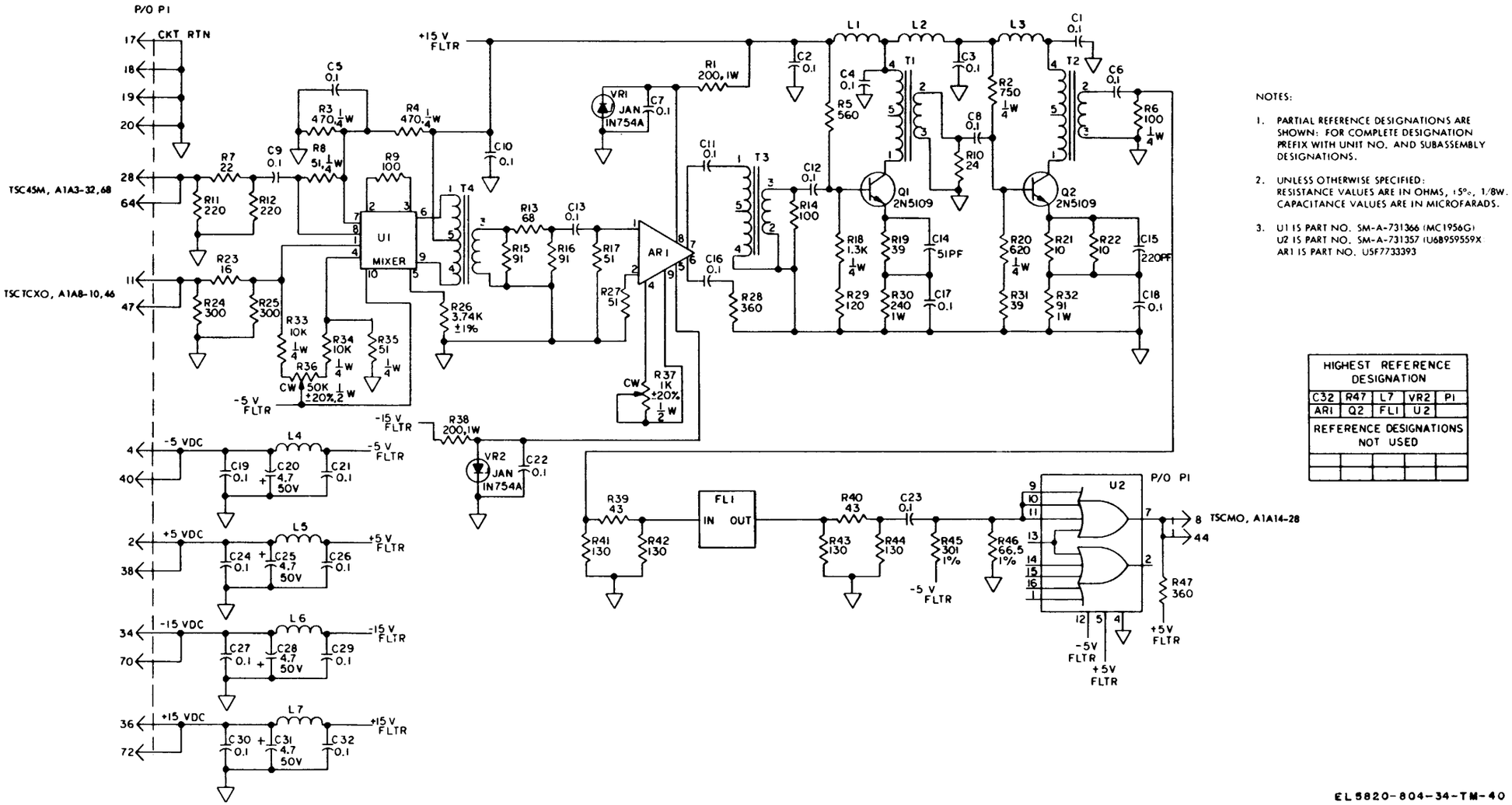


Figure FO-21. Stable clock, A2A1A1A12 (SM-D-731201) schematic diagram.

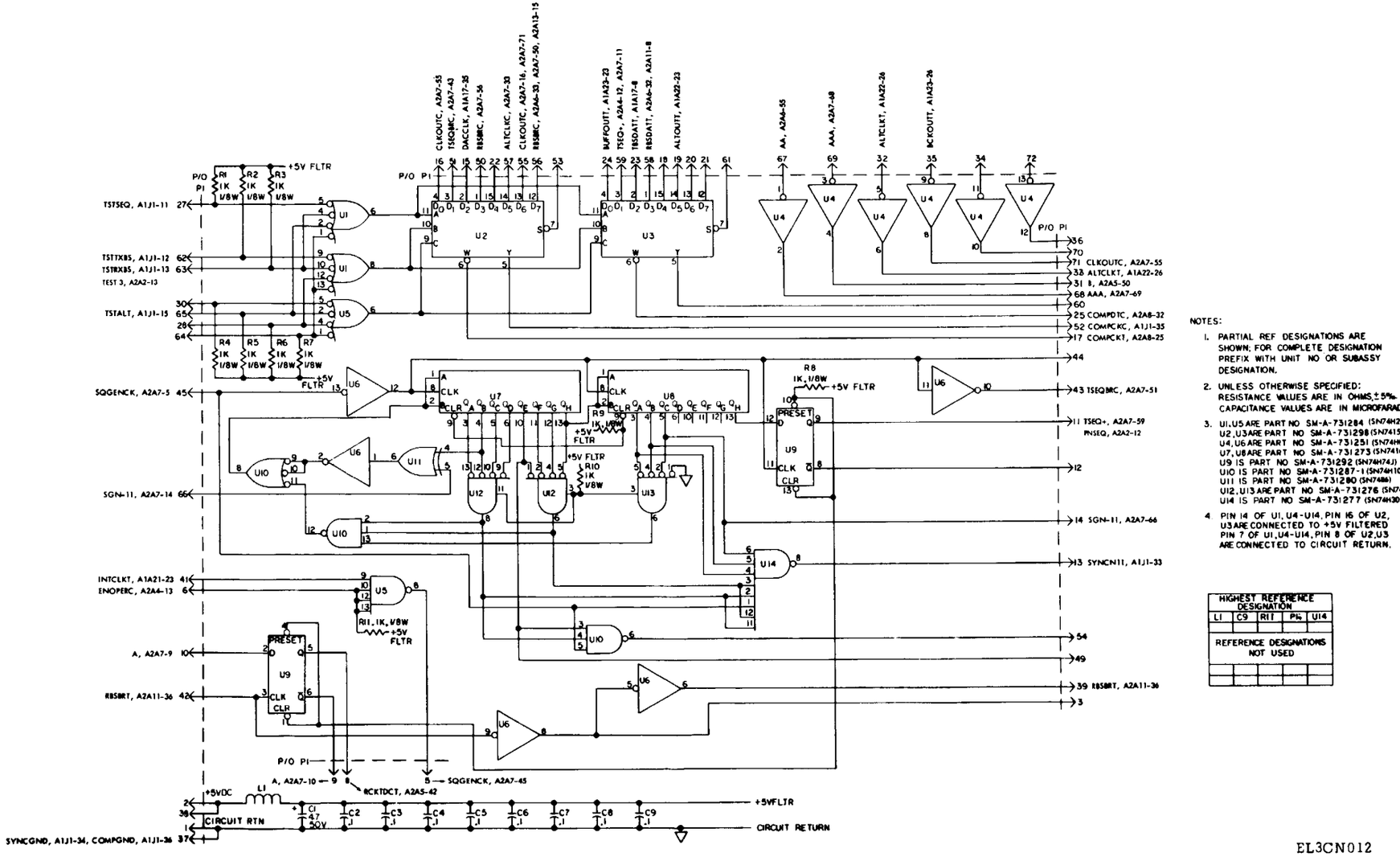
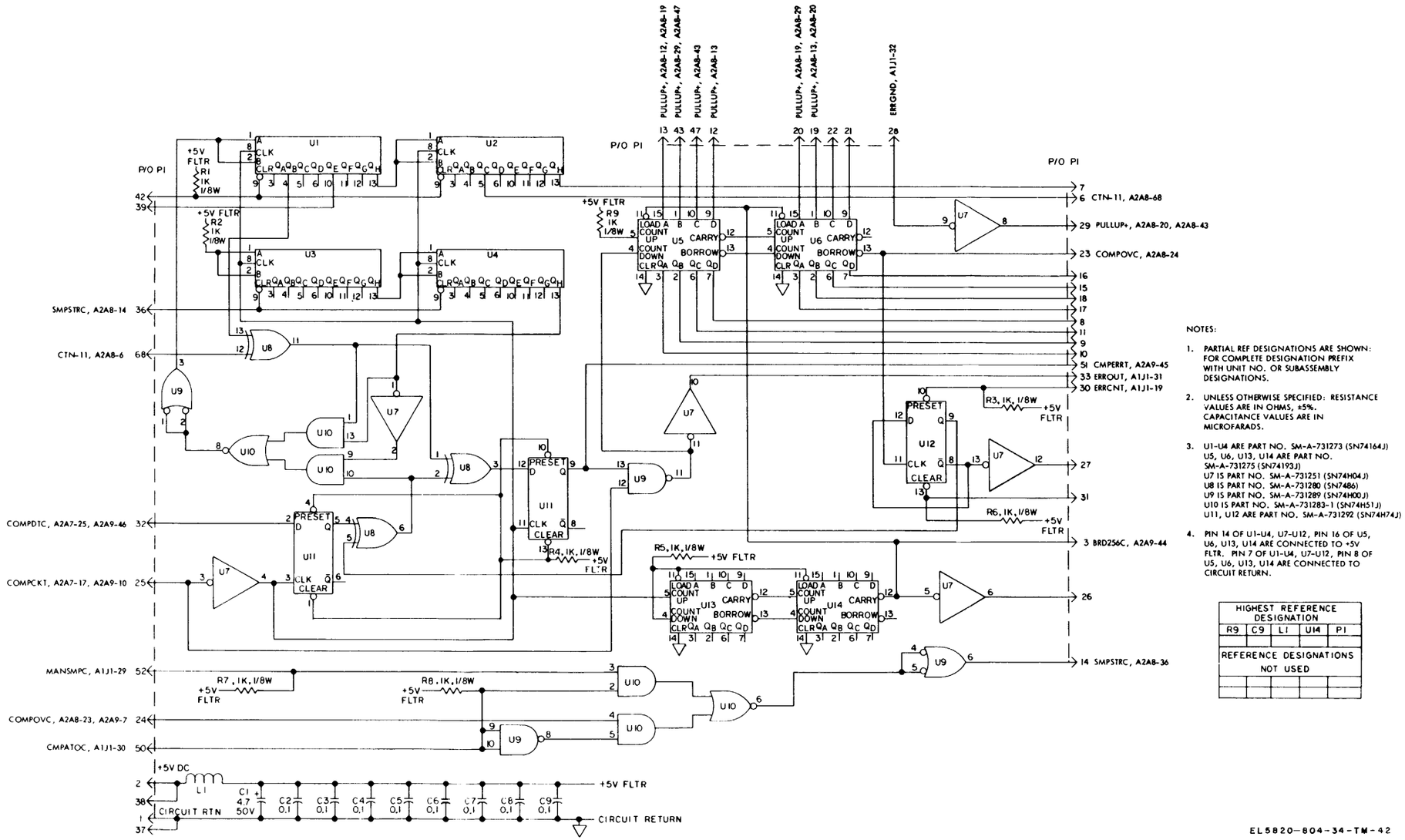


Figure FO-22. 11-bit PN sequence generator, A2A1A2A7 (SM-D-742057) schematic diagram.



NOTES:

1. PARTIAL REF DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSEMBLY DESIGNATIONS.
2. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, ±5%. CAPACITANCE VALUES ARE IN MICROFARADS.
3. U1-U4 ARE PART NO. SM-A-731273 (SN74164J)
   U5, U6, U13, U14 ARE PART NO. SM-A-731275 (SN74193J)
   U7 IS PART NO. SM-A-731251 (SN74H04J)
   U8 IS PART NO. SM-A-731280 (SN7486)
   U9 IS PART NO. SM-A-731289 (SN74H00J)
   U10 IS PART NO. SM-A-731283-1 (SN74H51J)
   U11, U12 ARE PART NO. SM-A-731292 (SN74H74J)
4. PIN 14 OF U1-U4, U7-U12, PIN 16 OF U5, U6, U13, U14 ARE CONNECTED TO +5V FLTR. PIN 7 OF U1-U4, U7-U12, PIN 8 OF U5, U6, U13, U14 ARE CONNECTED TO CIRCUIT RETURN.

HIGHEST REFERENCE DESIGNATION				
R9	C9	L1	U14	P1
REFERENCE DESIGNATIONS NOT USED				

EL5820-804-34-TM-42

Figure FO-23. Error comparator, A2A1A2A8 (SM-D-742061) schematic diagram.

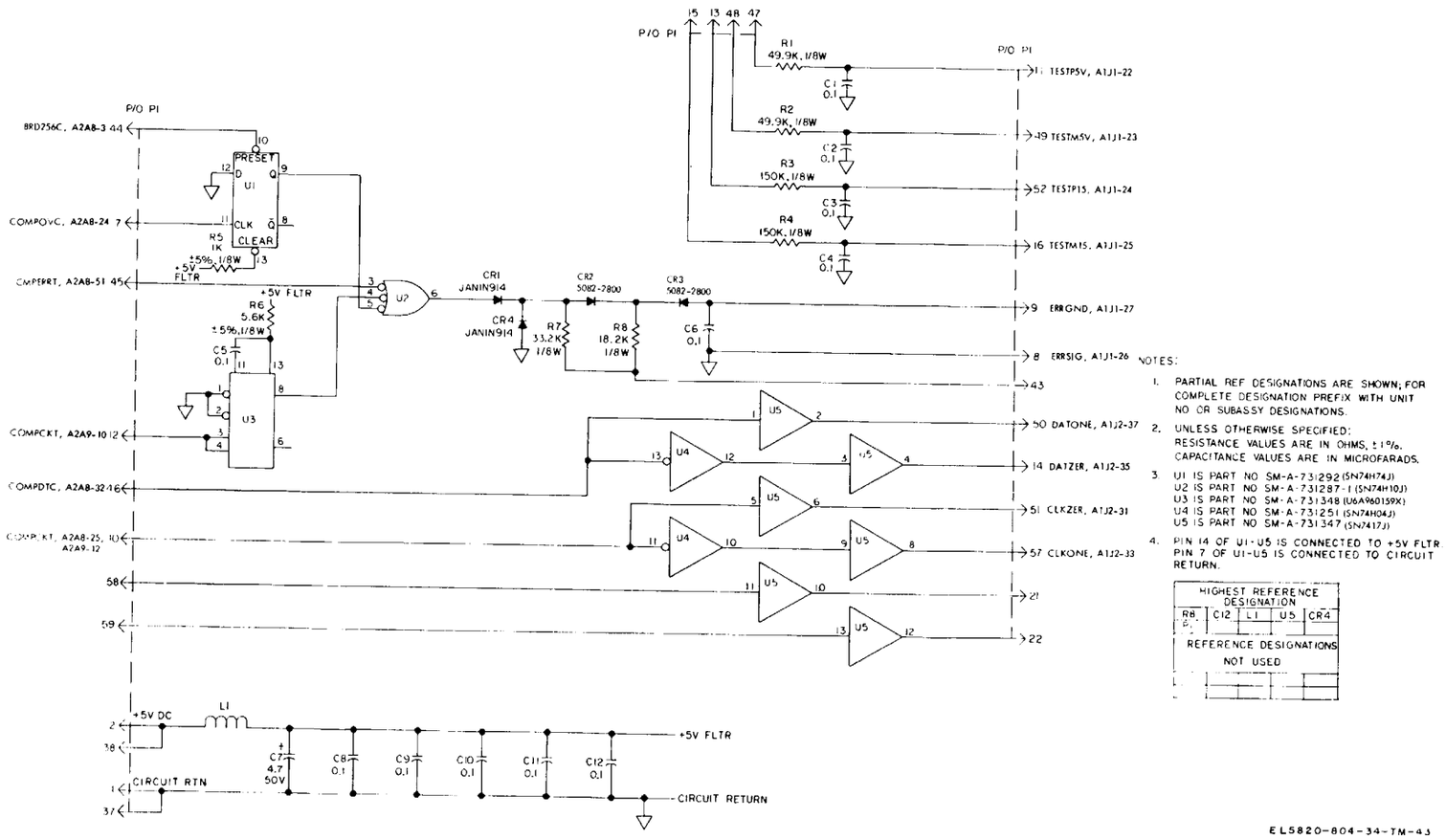


Figure FO-24. Digital-to-analog meter, A2A1A2A9 (SM-D-742065) schematic diagram.

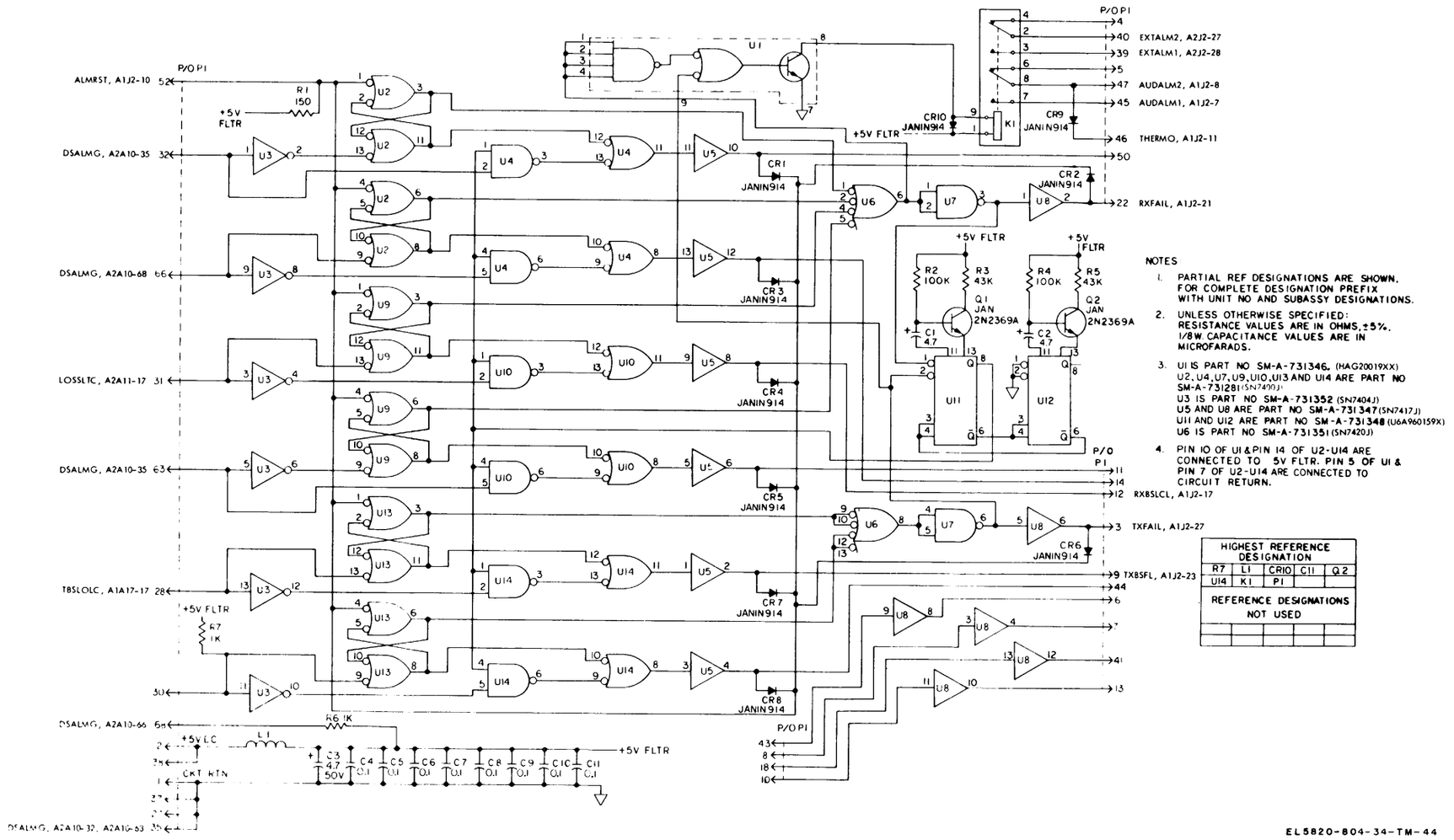


Figure FO-25. Alarm circuits, A2A1A2A10 (SM-D-742033) schematic diagram.

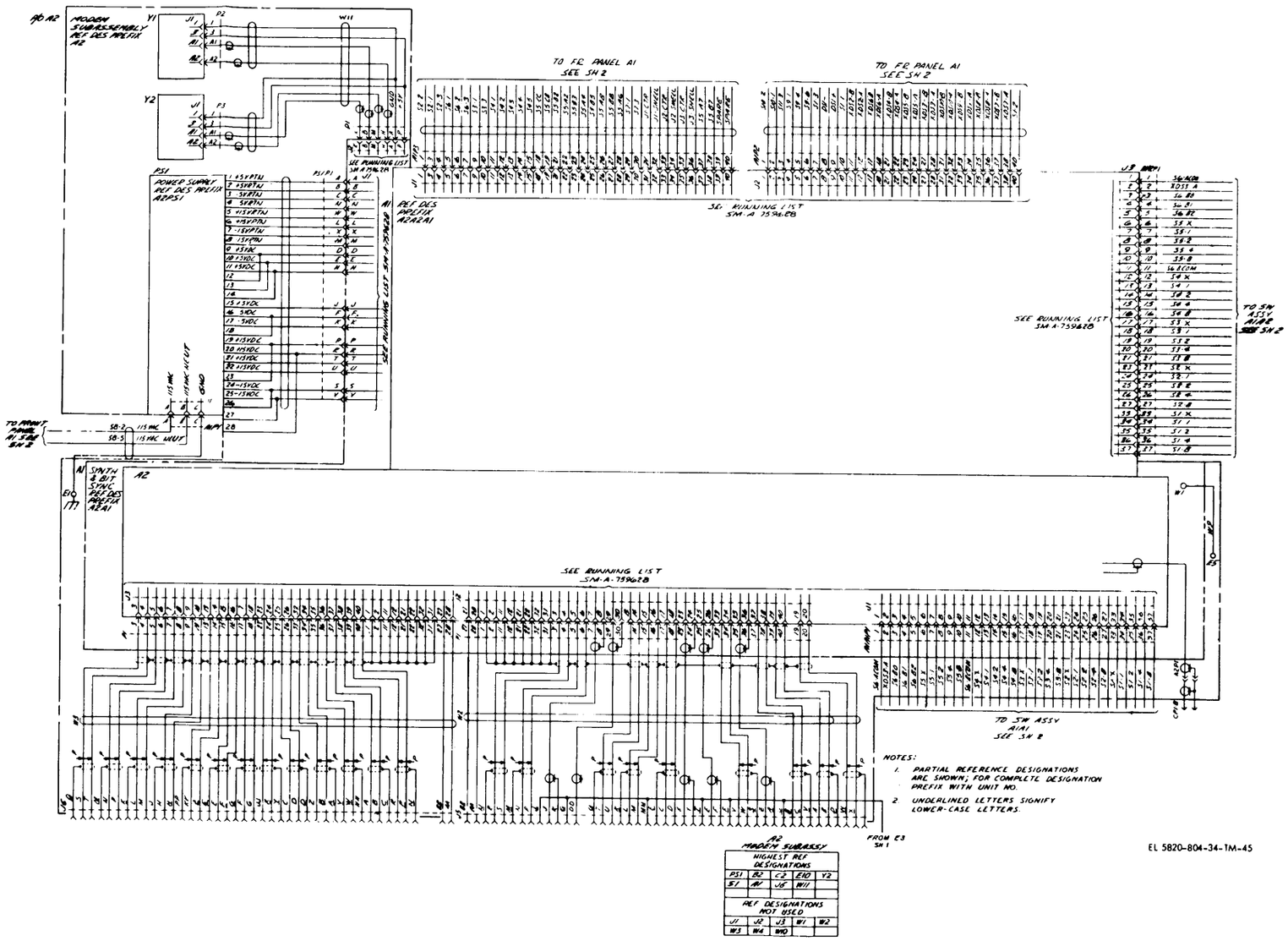


Figure FO-26. (1). ICF modem, interconnection diagram (sheet 1 of 2)

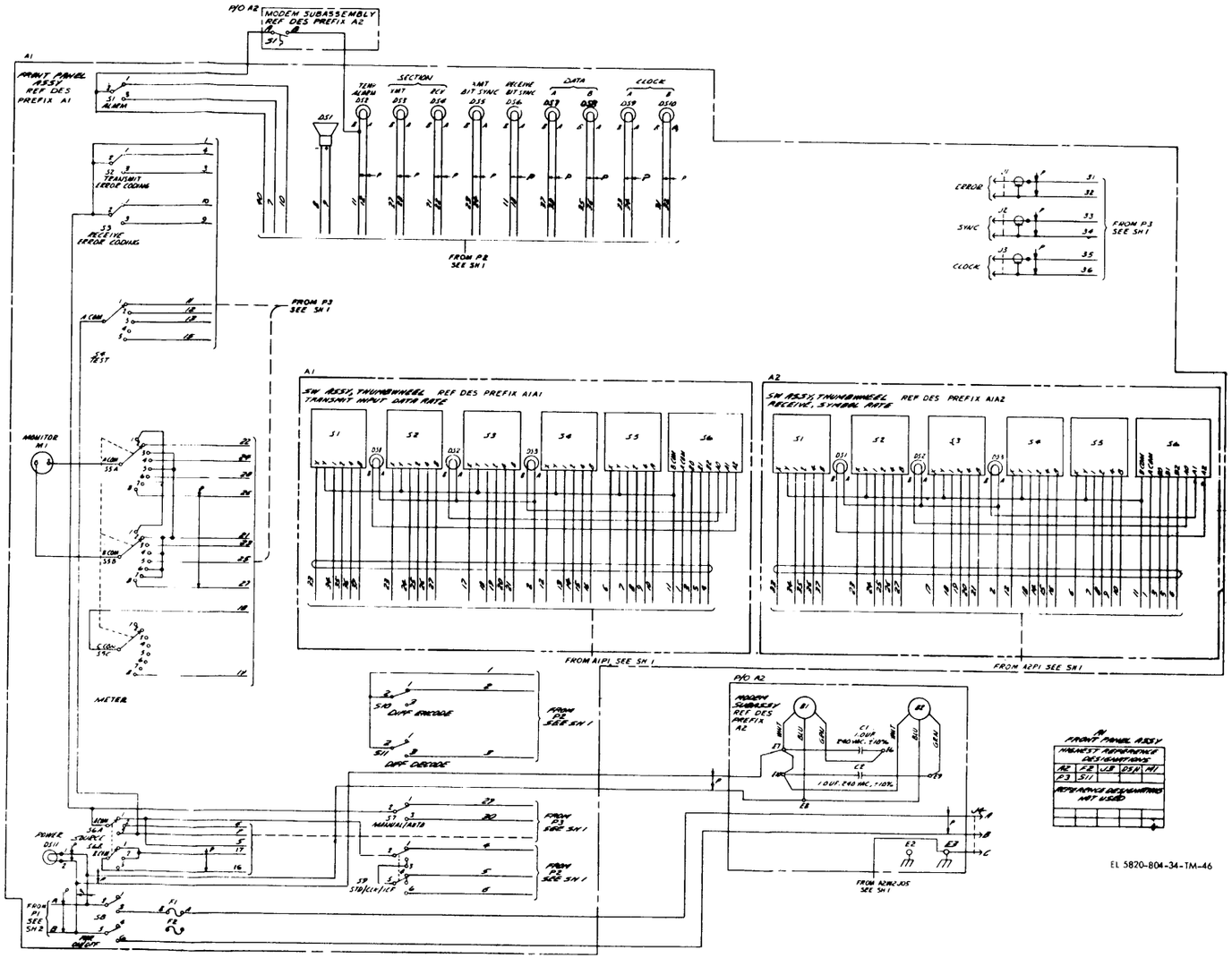
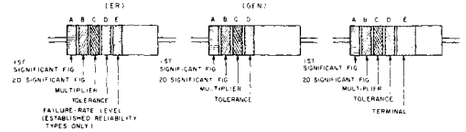


Figure FO-26 (2). ICF modem, interconnection diagram (sheet 2 of 2)



COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS

COLOR CODE MARKING FOR FILM-TYPE RESISTORS

TABLE I
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM
BLACK	0	BLACK	0	BLACK	1			BROWN	M 1.0	
BROWN	1	BROWN	1	BROWN	10			RED	P .01	
RED	2	RED	2	RED	100			ORANGE	R .001	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S .0001	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP. TYPE ONLY) ±5	WHITE		SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)			
BLUE	6	BLUE	6	BLUE	1,000,000	RED				
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	0.01					
WHITE	9	WHITE	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE - RATE LEVEL (PERCENT FAILURE PER 1000 HOURS). ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1½ TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL.

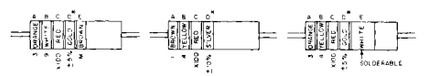
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODED.)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE

2R7 = 2.7 OHMS 10R0 = 10.0 OHMS

FOR WIRE WOUND-TYPE RESISTORS COLOR CODING IS NOT USED. IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 3300 OHMS
RESISTANCE TOLERANCE ±5%
FAILURE RATE LEVEL M

NOMINAL RESISTANCE 1400 OHMS
RESISTANCE TOLERANCE ±10%

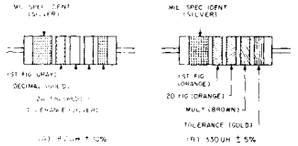
NOMINAL RESISTANCE 3400 OHMS
RESISTANCE TOLERANCE ±5%
TERMINAL SOLDERABLE

COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD

A COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS



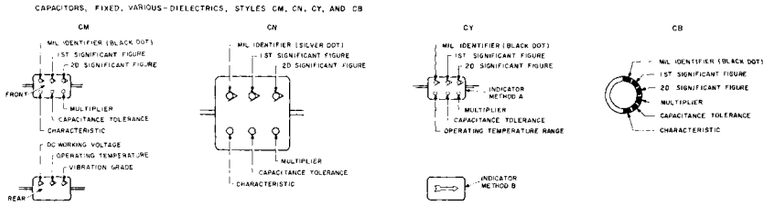
COLOR CODING FOR TUBULAR ENCAPSULATED RF CHOKES AS AN EXAMPLE OF THE CODING FOR AN 8.2 UH CHOKE IS GIVEN AT A, THE COLOR BANDS FOR A 330 UH INDUCTOR ARE ILLUSTRATED

TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED RF CHOKES

COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	10²	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE (UH).

B COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS.



C COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS

TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB.

COLOR	MIL ID	1ST SIG FIG	2D SIG FIG	MULTIPLIER	CAPACITANCE TOLERANCE CM	CN	CY	CB	CHARACTERISTIC CM	CN	CB	DC WORKING VOLTAGE CM	OPERATING TEMP RANGE CY, CM	VIBRATION GRADE CM
BLACK	CM, CY, CB	0	0	1			±20%	±20%	A				-55°_{+10} +70°C	10-55 HZ
BROWN		1	1	10					B	E	B			
RED		2	2	100	±2%		±2%	±2%	C				-55°_{+10} +85°C	
ORANGE		3	3	1,000	±30%				D		D	300		
YELLOW		4	4	10,000					E				-55°_{+10} +125°C	10-2,000 HZ
GREEN		5	5		±5%				F			500		
BLUE		6	8										-55°_{+10} +150°C	
PURPLE (VIOLET)		7	7											
GRAY		8	8											
WHITE		9	9											
GOLD				0.1			±5%	±5%						
SILVER	CN			0.01	±10%		±10%	±10%						

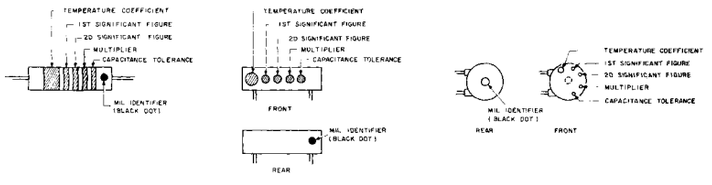


TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC.

COLOR	TEMPERATURE COEFFICIENT 4	1ST SIG FIG	2D SIG FIG	MULTIPLIER 1	CAPACITANCE TOLERANCE: CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	MIL ID
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	−30	1	1	10	±1%		
RED	−80	2	2	100	±2%	±0.25 UUF	
ORANGE	−150	3	3	1,000			
YELLOW	−220	4	4				
GREEN	−330	5	5		±5%	±0.5 UUF	
BLUE	−470	6	6				
PURPLE (VIOLET)	−750	7	7				
GRAY		8	8	0.01*			
WHITE		9	9	0.1*	±10%		
GOLD	+100			0.1		±1.0 UUF	
SILVER				0.01			

1 THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.

2 LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS MIL-C-5, MIL-C-20, MIL-C-11272B, AND MIL-C-11015C RESPECTIVELY.

3 LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D.

4 TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE

* OPTIONAL CODING WHERE METALLIC PIGMENTS ARE UNDESIRABLE.

ESC FM 913 73

Figure FO-27. Color code marking for military standard resistors. Inductors and capacitors.

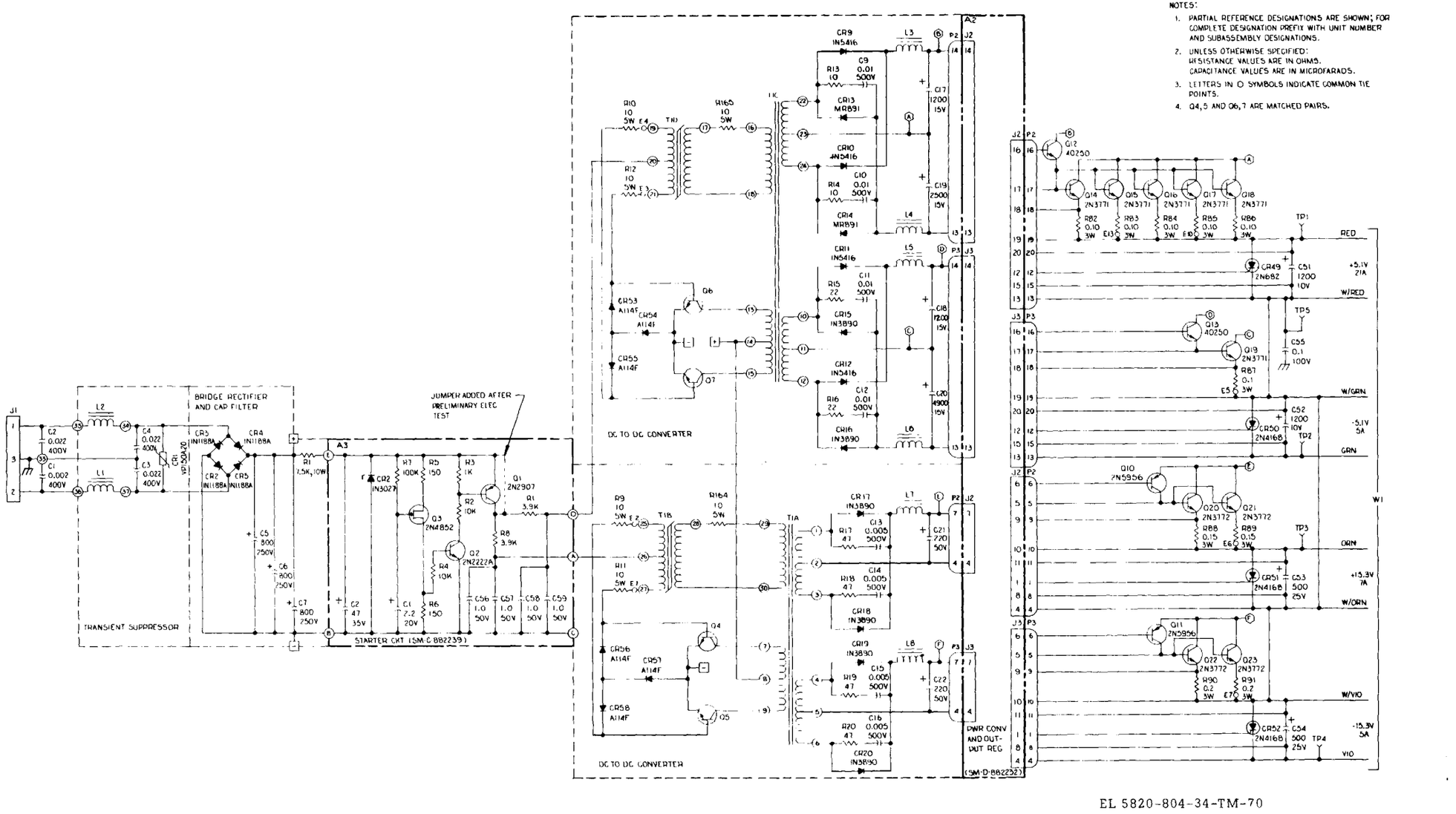


Figure FO-28. Power supply PS1 (SM-C-759630), schematic diagram.

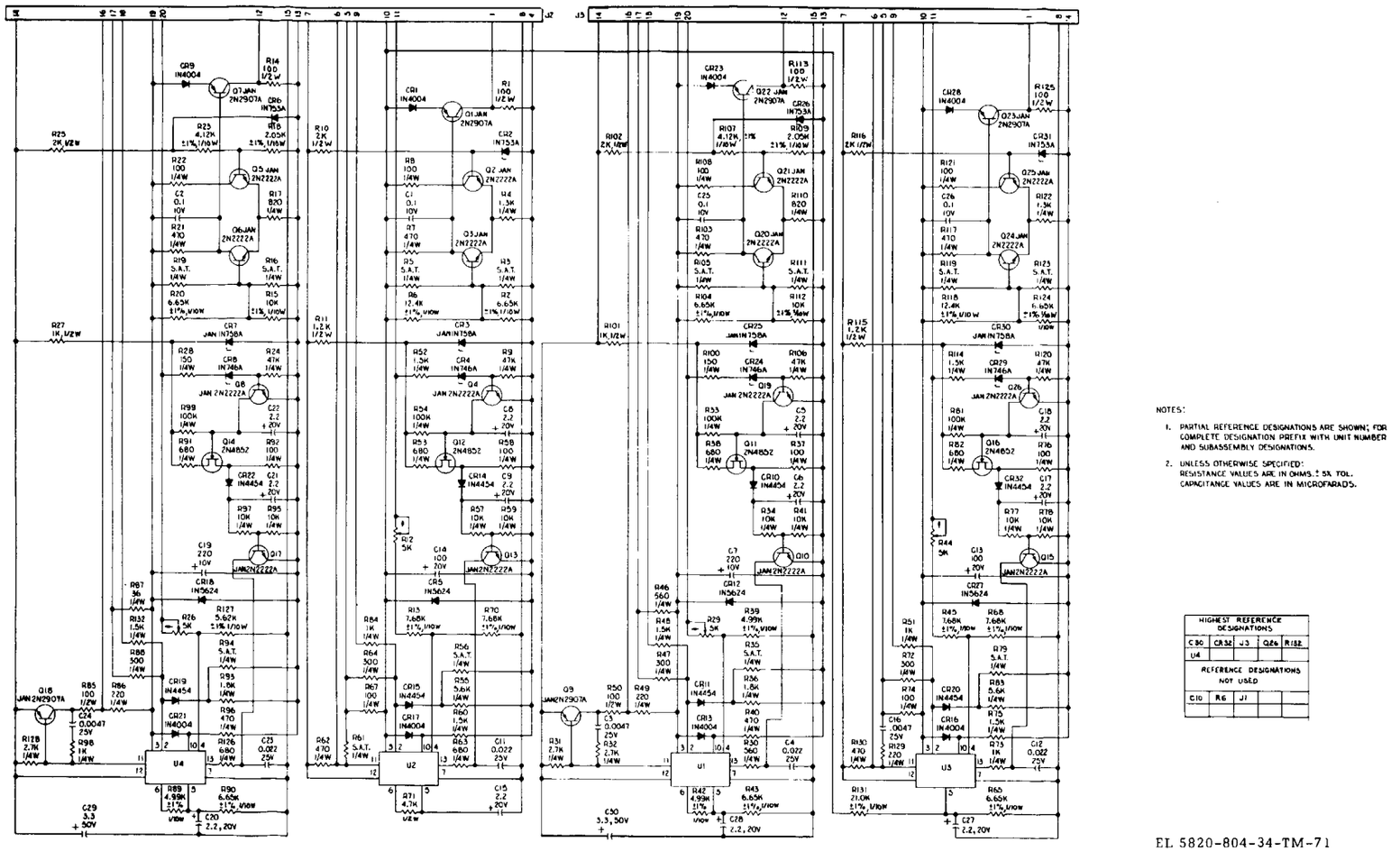


Figure FO-29. Power supply PSI, assembly A2 (SM-D-882232), schematic diagram.

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